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SIMULATION OF LOW POWER 16-BIT PROCESSOR USING CADENCE - 45nm FOUNDRY TECHNOLOGY

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ABSTRACT

In the era of wearable devices, there is an increasing demand for energy-efficient solutions to prolong battery life and reduce environmental impact. This work focuses on the design and implementation of low-power techniques of 16-bit processor that can be specifically tailored for IoT applications. This research presents a comprehensive exploration of the design and implementation of a 16-bit processor utilizing 45nm semiconductor technology. The design process begins with a detailed analysis of the 16-bit processor architecture, considering key components such as the Arithmetic Logic Unit, Register file, Instruction register, Mux, PC, Data Path and Controller subsystem. A systematic approach is employed to optimize critical pathways ensuring efficient data flow and reduced signal propagation delays. To leverage the benefits of 45nm technology, the design incorporates smaller feature sizes, enabling higher transistor density and improved energy efficiency. Cadence synthesis and optimization tools are employed to refine the design, considering factors such as transistor sizing, interconnect optimization, and layout considerations. The introduction of clock domain crossing mechanisms plays a pivotal role in power reduction. By dynamically controlling the 100MHz clock signals to specific modules based on their operational requirements, power consumption is significantly lowered during periods of inactivity. The design also explores trade-offs between power savings and potential impacts on performance, ensuring a balanced and efficient system. Simulation results and performance metrics are presented to validate the effectiveness of the proposed 16-bit processor design. This research contributes to the ongoing efforts in developing energy-efficient processors, providing valuable insights into the synergies between advanced semiconductor technologies and power optimization techniques. The findings are relevant for the design and implementation of processors in applications where power efficiency is a critical consideration, such as IoT based portable devices and energy-constrained environments. The power dissipation using 45nm is 739456.21020nw for full-data path with 5925 instances & 201625.2594nw for controller with 222 cells.

Keywords: Low Power, 16-bit Processor, 45nm, Power dissipation, Dynamic-power, Static-Power, CDC.

1. INTRODUCTION

Design of Processor is always essential, due to its extensive usage. Of all 16-bit processors are important in embedded systems due to their versatility, cost-effectiveness, power efficiency, and suitability for a wide range of applications spanning industries such as automotive, medical, consumer electronics, and IoT. Their adoption continues to thrive as technology evolves and demands for efficient embedded solutions persist across various domains that provide the balance between performance, power efficiency, and cost. 16-bit processors are often

more cost-effective compared to higher-bit processors. They provide a good balance between performance and cost, making them suitable for applications with budget constraints, such as consumer electronics and low-cost embedded systems. 16-bit processors typically consume less power compared to higher-bit processors. This makes them suitable for battery-powered devices and applications where power efficiency is critical, such as portable devices, IoT nodes, and sensor nodes. Many embedded systems require real-time processing capabilities, such as in control systems, automotive applications, and industrial automation. The simplicity and efficiency of 16-bit processors make them well-suited for real-time applications where quick decision-making and response times are essential. 16-bit processors often come with integrated peripherals and interfaces, simplifying the design of embedded systems. This integration reduces the need for additional components, leading to a more compact and cost-effective overall system. In applications where communication and connectivity are key, such as in networking devices and communication modules, 16-bit processors provide sufficient processing power to handle data transfer and protocol handling while maintaining a reasonable level of energy efficiency. In the automotive industry, 16-bit processors are commonly used in various control units, including engine control units (ECUs), airbag systems, and anti-lock braking systems (ABS). Their real-time processing capabilities are well-suited for controlling critical functions in vehicles. 16-bit processors are employed in medical devices, including portable diagnostic tools, patient monitoring systems, and infusion pumps. The combination of processing power, low power consumption, and cost-effectiveness makes them ideal for medical applications. In consumer electronics, 16-bit processors are often found in devices such as digital cameras, handheld gaming consoles, and home appliances. Their cost-effectiveness and power efficiency contribute to the widespread use in these applications. With the growing prevalence of IoT, 16-bit processors are used in various IoT devices, including smart sensors, wearable's, and home automation systems. Their ability to perform basic tasks efficiently aligns well with the requirements of many IoT applications. The Design Metrics collectively provide a comprehensive view of a processor's performance, balancing speed, power efficiency, and resource utilization. Designers often optimize these metrics based on the specific requirements of the target application and the constraints of the embedded system. key metrics used to evaluate the performance of a processor are stated below Clock Frequency, the clock frequency, measured in Hertz (Hz) or megahertz (MHz), represents the rate at which the processor's internal operations are synchronized. Higher clock frequencies generally indicate faster processing capabilities. However, it's crucial to consider power consumption and heat dissipation, as increasing clock frequency may lead to higher power requirements. Throughput, the throughput measures the amount of data processed per unit of time and is often expressed in bits per second (bps) or transactions per second (TPS). Throughput provides a broader perspective on the processor's overall performance, considering both the clock frequency and the efficiency of instruction execution. IPC represents the average number of instructions executed per clock cycle. A higher IPC value indicates better efficiency in executing instructions, which can contribute to improved performance without solely relying on increased clock frequencies. Power consumption measures the amount of electrical power consumed by the processor during operation and is often expressed in watts (W). Low power consumption is critical for battery-powered devices and applications where energy efficiency is a priority. Power efficiency is evaluated across different operational states, including active, idle, and sleep modes. Energy efficiency is a measure of how effectively the processor performs computations while minimizing power consumption. It combines performance and power consumption metrics to assess how much energy is used to complete a specific task. Energy efficiency is crucial for portable and battery-operated devices. Area utilization measures the physical size of the processor on the chip and is often expressed in square millimeters. Efficient use of silicon real estate is important for cost-effective designs. Smaller processors with optimized layouts can contribute to reduced manufacturing costs and increased integration possibilities. CPI measures the average number of clock cycles required to execute one instruction. A lower CPI indicates better efficiency in instruction execution. CPI is closely related to IPC and helps assess how well the processor utilizes each clock cycle. Cache performance metrics include hit rate, miss rate, and latency in accessing the cache memory. Cache efficiency impacts overall processor performance. Higher hit rates and lower miss rates contribute to improved performance by reducing memory access latency. Latency measures the time delay between initiating a process and receiving the result, while

response time is the total time taken to complete a task. Low latency and response times are critical in real-time applications, ensuring quick decision-making and responsiveness. FLOPS measures the number of floating-point operations a processor can perform in one second. FLOPS are crucial for applications requiring extensive floating-point calculations, such as scientific simulations and graphics processing. Clock Domain Crossing (CDC) is a crucial aspect in the design and verification of digital integrated circuits, especially in Very Large Scale Integration (VLSI) designs. In VLSI, a digital system often consists of multiple clock domains, each driven by its own clock signal. Clock domains are distinct regions of a design where the timing is controlled by a specific clock signal. Clock Domain Crossing occurs when signals or data cross between different clock domains. Managing this crossing is challenging because the clocks in different domains may have different frequencies, phases, or even be asynchronous. If not handled properly, CDC issues can lead to data synchronization problems, metastability, and ultimately impact the reliability and functionality of the digital system. When a signal crosses from one clock domain to another and violates the setup or hold time requirements, it can enter a metastable state. Metastability is an unpredictable state that can lead to incorrect data values and potentially cause the failure of the digital system. To mitigate the effects of metastability, synchronization elements such as flip-flops or double-flop synchronizers are often employed. These elements help in ensuring that data transitions between clock domains are captured reliably. Static timing analysis and formal verification are used to analyze and address CDC issues during the design and verification phases. The overall flow the work is mentioned as stated below.

Second section literature survey is conferred, third section exhibits about the proposed design, fourth section infers about obtained simulated results followed by conclusion and future scope.

2. LITERATURE SURVEY

Most of the authors have emphasized on the clock gating scheme and the design of 16-bit processors, here are few representations about them. In [1] year 2017, T.C. Taranth et.al signified about the RTL synthesis using Cadence DC. In [2] year 2021, M. W. El-Kharashi et.al focused on Open Lane and Commercial Approaches in Comparison with RISC processor. In [3] 2018, Technology mediated tutorial on RISCV CPU core implementation and sign-off using revolutionary EDA management system. In [4] 2014, N Saraswati et.al, has presented Cadence based Implementation of a 32-bit MIPS. In [5] 2012, Sangmin Kim et.al, have shown the synthesis of pulsed circuits using clock gating. In [6], the authors have analysed the 16-bit ALU with clock gating technique. In [7], the authors have simulated the 16bit processor using clock-gating technique with cadence 45nm technology. In [8], the authors presented the simulation of 16-bit processor using cadence 90nm technology. In [9], Sudha et.al, have contributed the work on physical synthesis of 16-bit processor. In [10] Chandran Venkatesan et.al, have proposed the design of RISC processor using Harvard architecture. In [11] Dr. Sujatha have implemented the design of 32 bit RISC processor. In [12], the authors have simulated the work on 32bit non-pipelined processor using cadence

3. PROPOSED DESIGN

This section deals with the proposed ASM design methodology & block representation. The CPU architecture method can be divided into two parts, the controller and the data path. By separating these two parts, the architecture of the device is streamlined. This application-driven design specifies the Finite State Machine (FSM) that governs the data path by the instructions to be executed. As a result, the control unit may be configured as an FSM that drives the pipeline phases that transmit signals to the data path unit to execute the operation encoded in the instruction set.

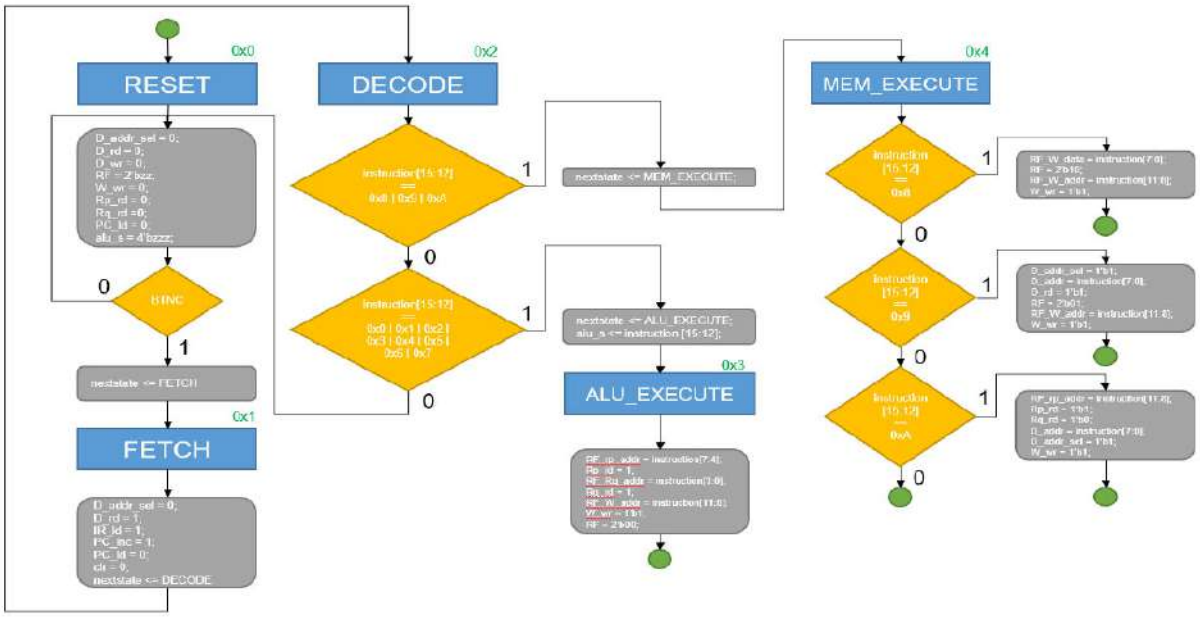

Fig A: Algorithmic State Machine.

The ASM Control Unit Map is presented in this section and was selected to present the architecture before the actions of the processor. Figure A indicates the ASM Chart Control Unit. There are 5 states in which the Control Unit cycles: Reset, Fetch, Decode, ALU Execute, and MEM Execute. The Reset state sets the control signals for both the Memory Unit and the Datapath Unit to 0. In this mode, the next state to prevent the program from cycling through all instructions without warning from the user. Next, the Retrieval State is present to recover the address from the Memory Unit and load it into the Instruction Register. After obtaining the address, the Control Unit will go to the Decode state where the Instruction will be evaluated for its opcode. Based on the opcode, the Control Unit assigns the next state either to the MEM Execute or to the ALU Execute states, the former to the load-store instructions, and the latter to the logical or arithmetic instructions. If the Control Unit runs between these two states, it returns to the Reset state and waits for the user to retrieve the next instruction.

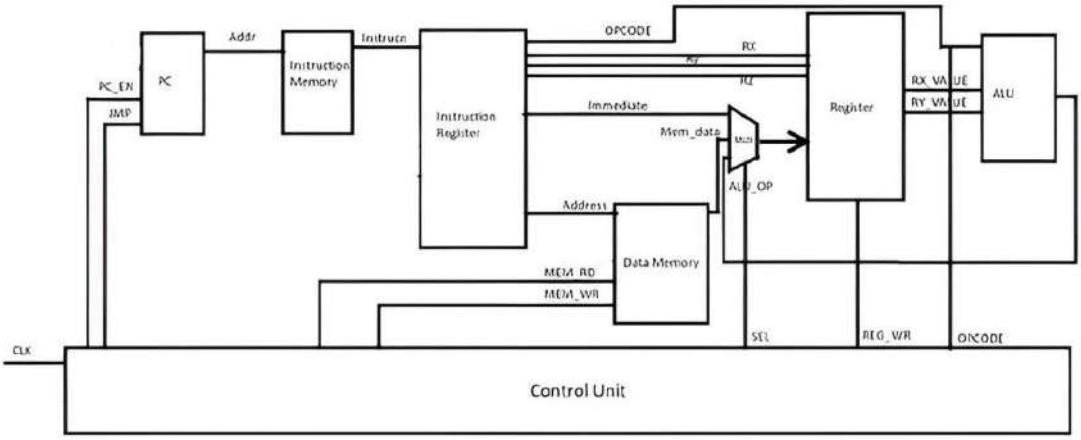

Fig B – Existing System Design[9]

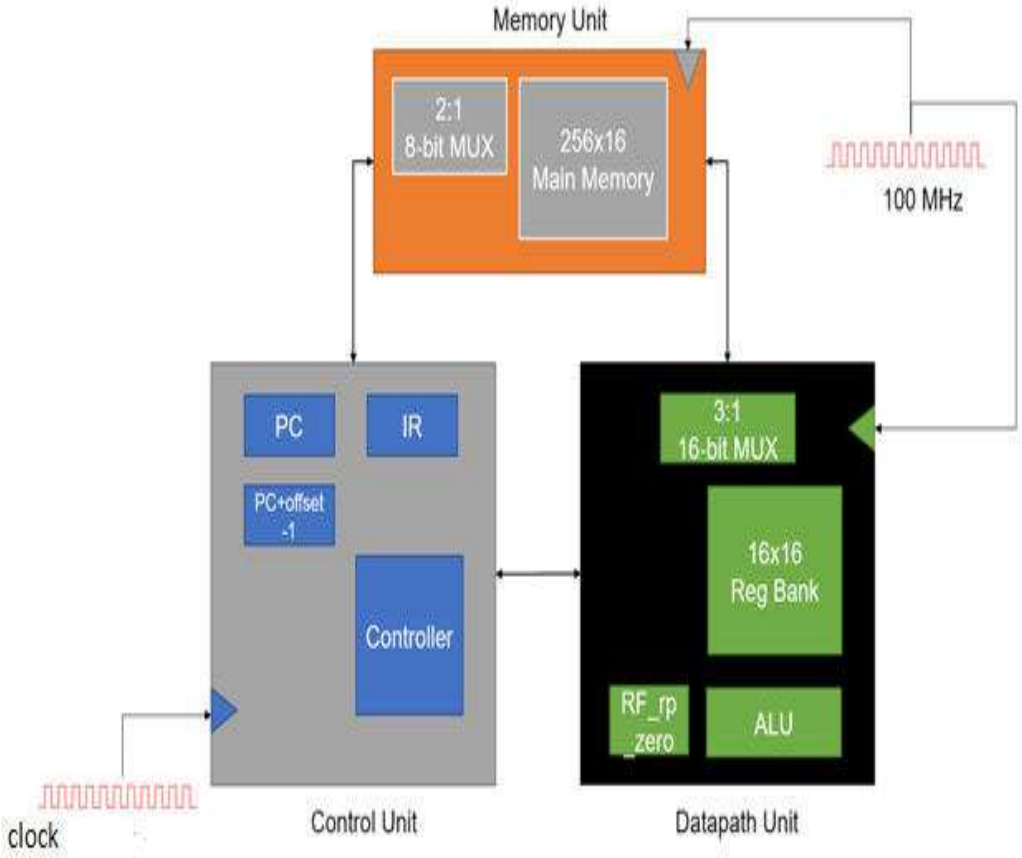

Fig C – Proposed Design of Control Unit, Memory Unit, Data path Unit

To simplify the architecture, the processor is divided into three different units: power, memory, and data path units. At a high stage, the control unit retrieves the instruction, decodes it, and sends the necessary signals to all memory and data path systems to execute the instruction. The data path unit controls access to the registry bank, performs arithmetic and logical operations, and communicates with all control and memory units. The memory unit manages access to the main memory and interacts with both control and data path drives. This high-level description is shown in Figure B and the HDL code represents this hierarchy as shown—the blocks within the units are sub modules to the unit module.

4. SIMULATION RESULTS:

As far as the difficulty of the configuration and execution of the Power, Datapath and Memory Units is concerned, the Control Unit was definitely the most difficult; the Memory Unit was the easiest and the Datapath Unit followed suit. First, all of the submodules, except the Controller, were designed and evaluated individually. After that, the design phase for the Memory and Datapath Systems was as follows: create and evaluate individual submodules within the Device, test the submodules in tandem, and eventually construct and test the submodule wrapper as a Device. Once the Datapath and Memory Modules were designed and tested separately, they were integrated and tested in unison. After testing the proper operation of both devices, the controller was modelled with the ASM chart displayed. Next, the HDL Controller was developed and simulated by linking the other two submodules in the Control Unit: the PC and the IR.

The next move with the Control Unit in service was to test it with the Memory Unit. The testing of the proper operation with the Datapath Unit was carried out following the Memory Unit evaluation. The Processor was eventually designed as the top module containing the Power, Memory, and Datapath Modules.

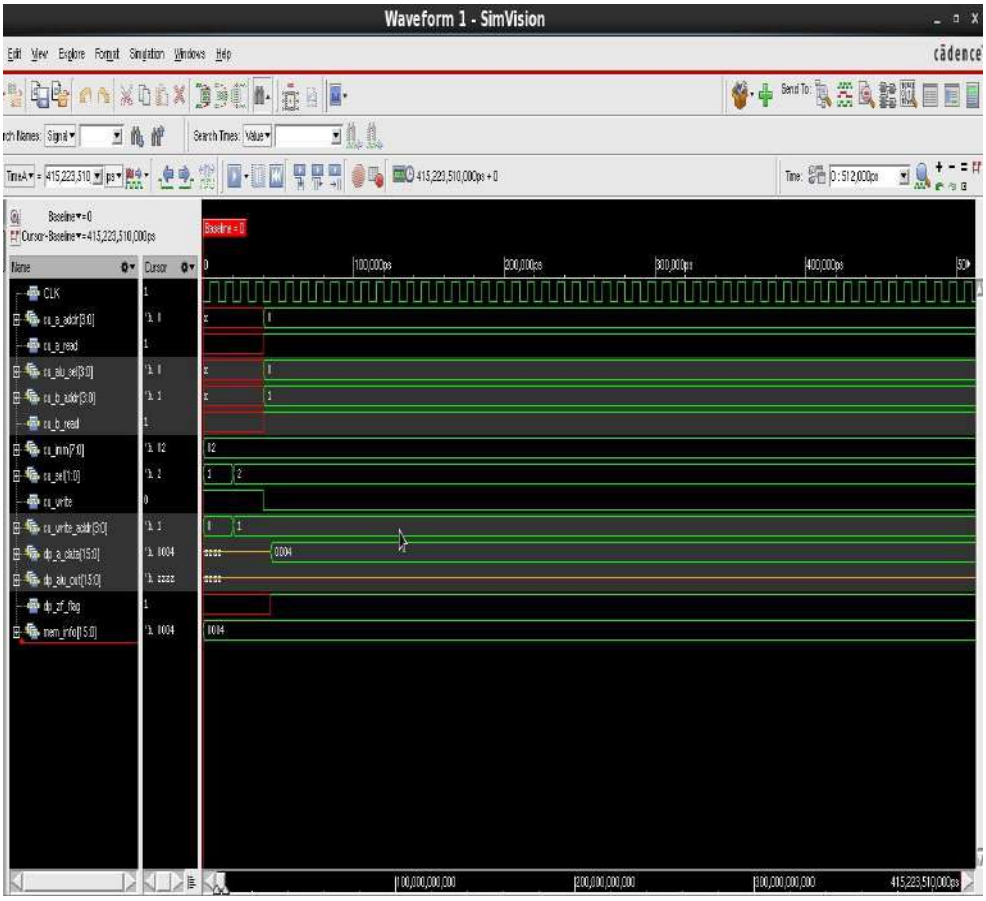

Fig 1: Simulation of Datapath

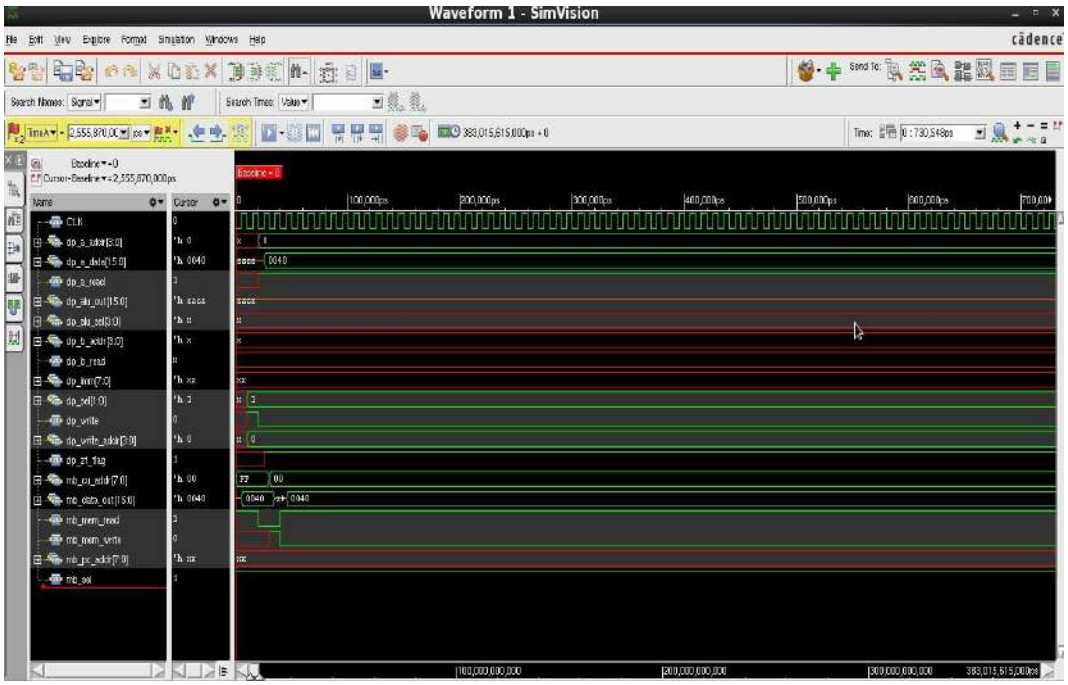

Fig 2: Simulation of Full Datapath

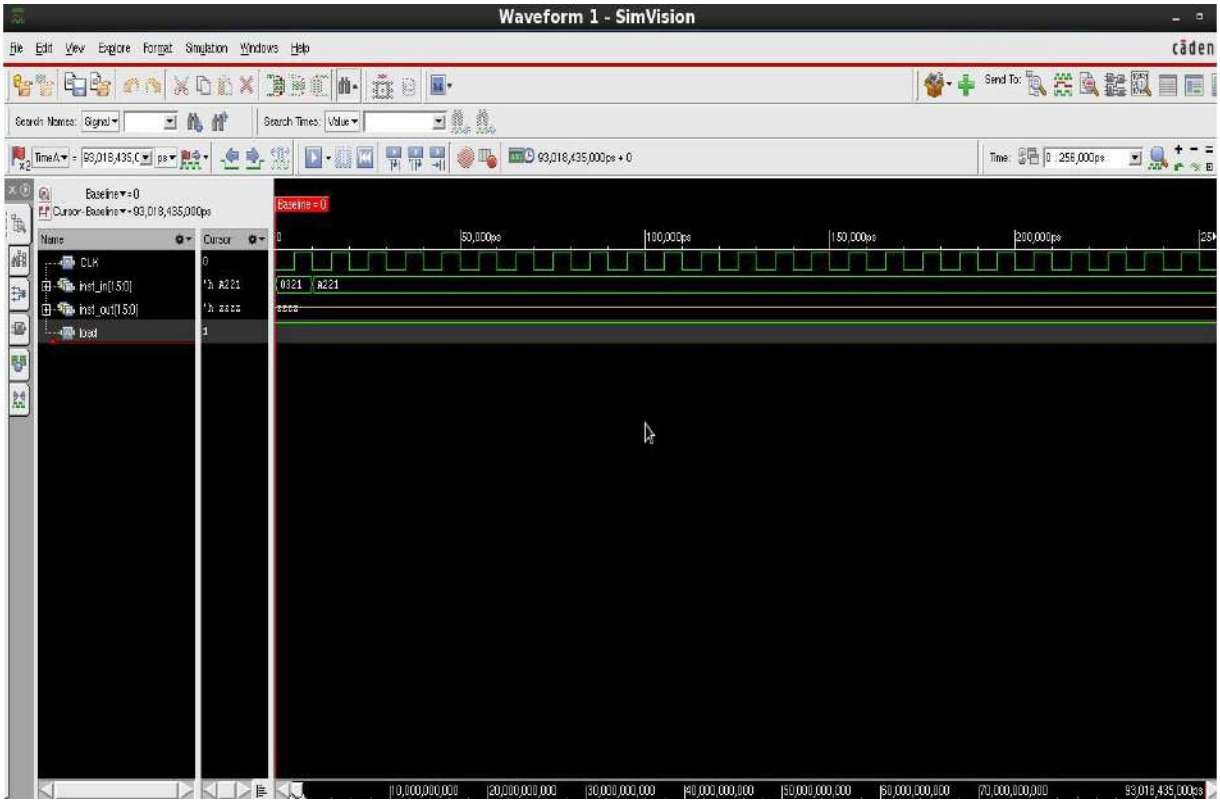

Fig 3: Simulation of IR

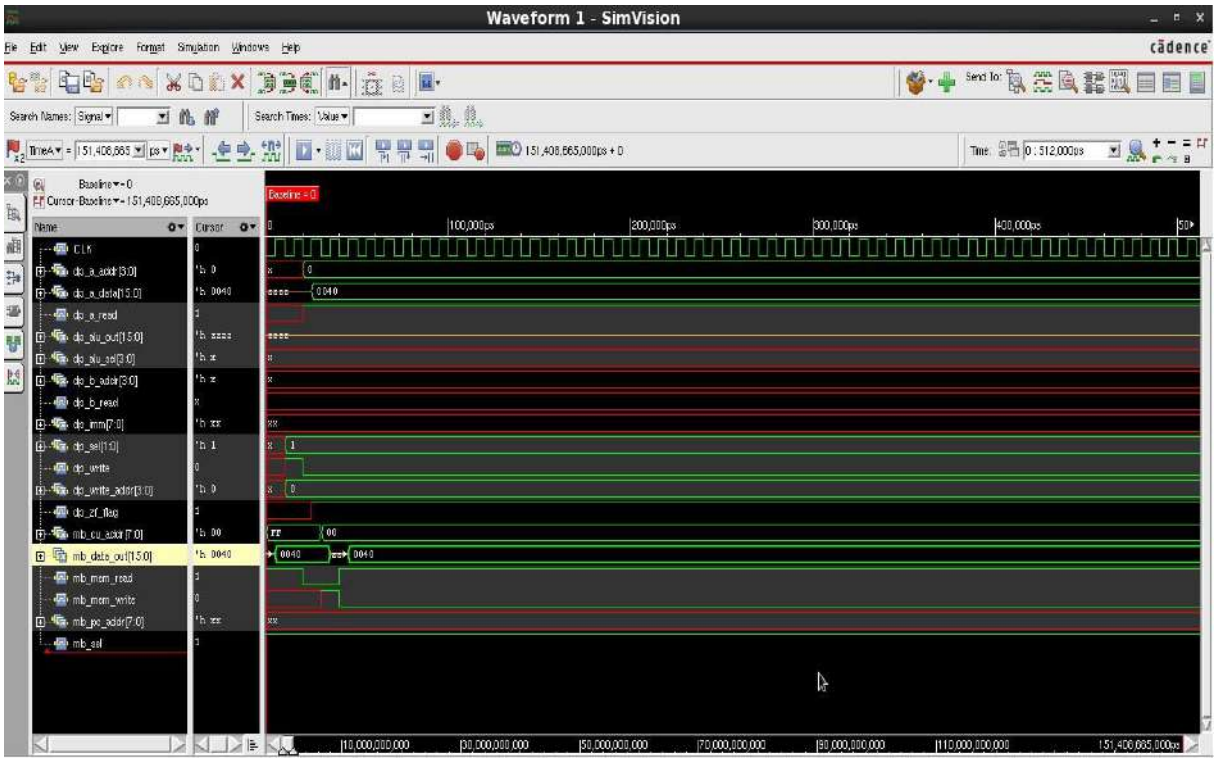

Fig 4: Simulation of Mem_dp

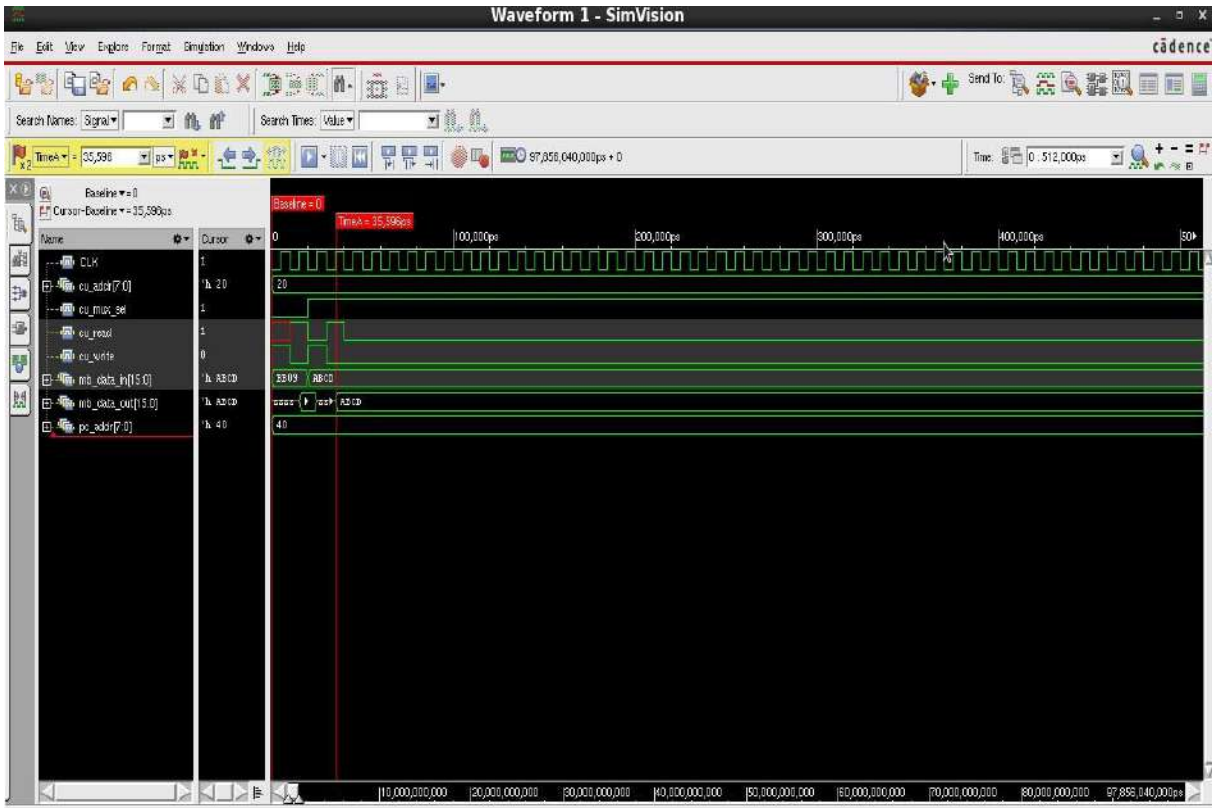

Fig 5: Simulation of Memory

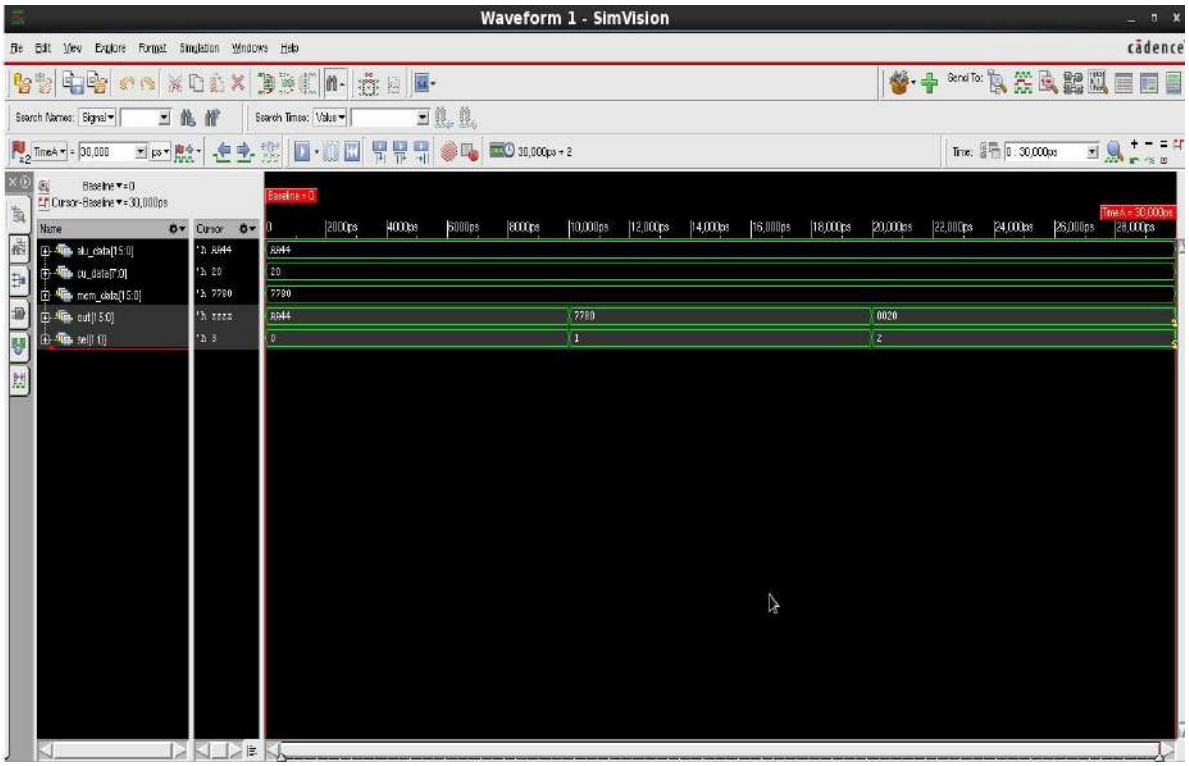

Fig 6: Simulation of Mux Data Path

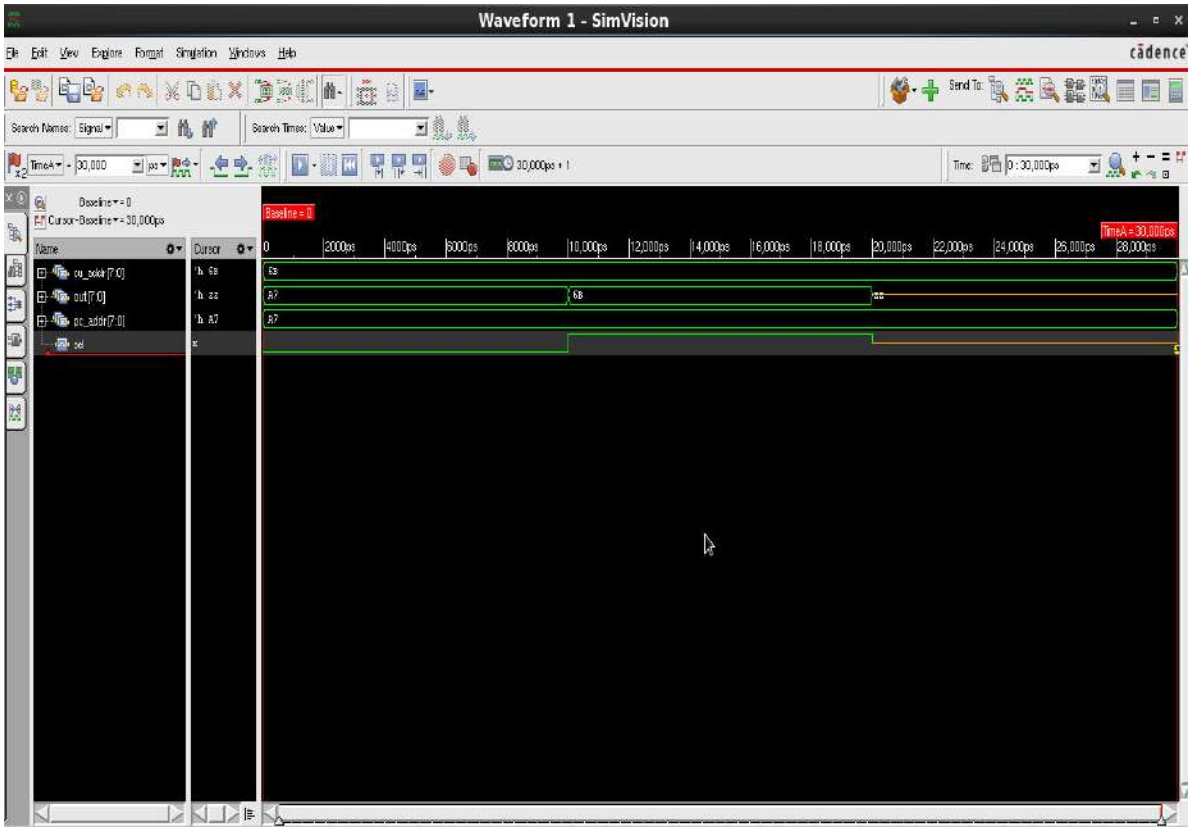

Fig 7: Simulation of Mux Mem

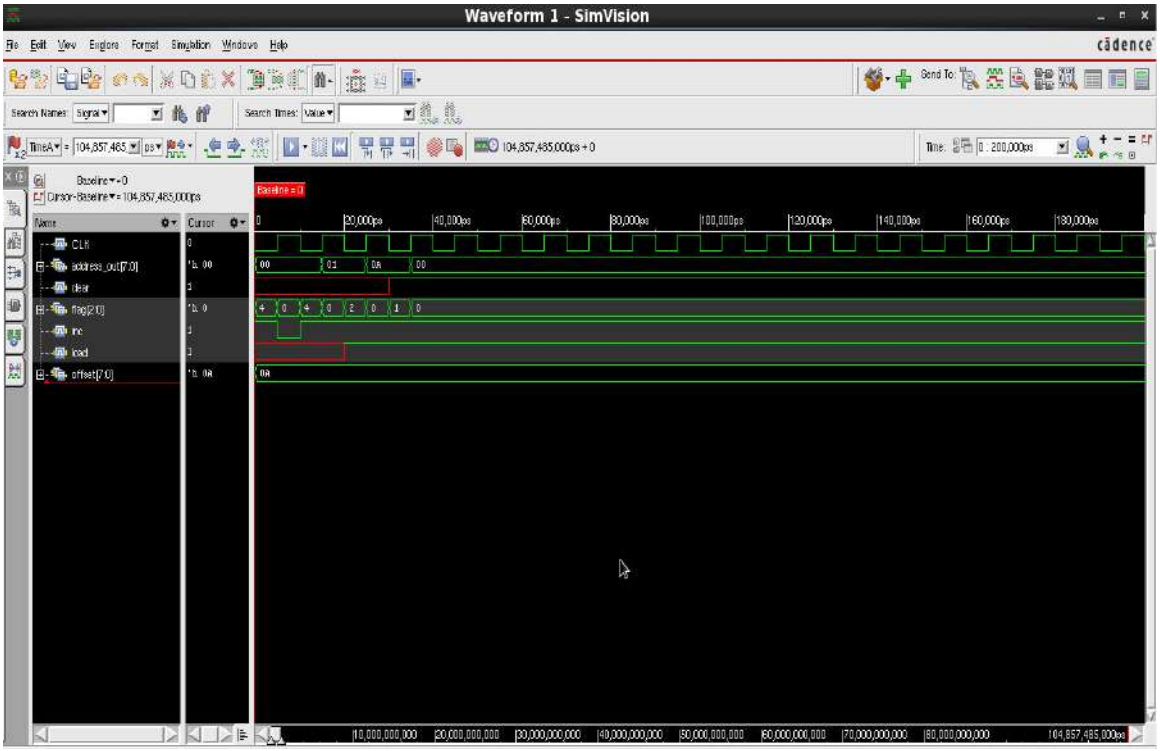

Fig 8: Simulation of PC

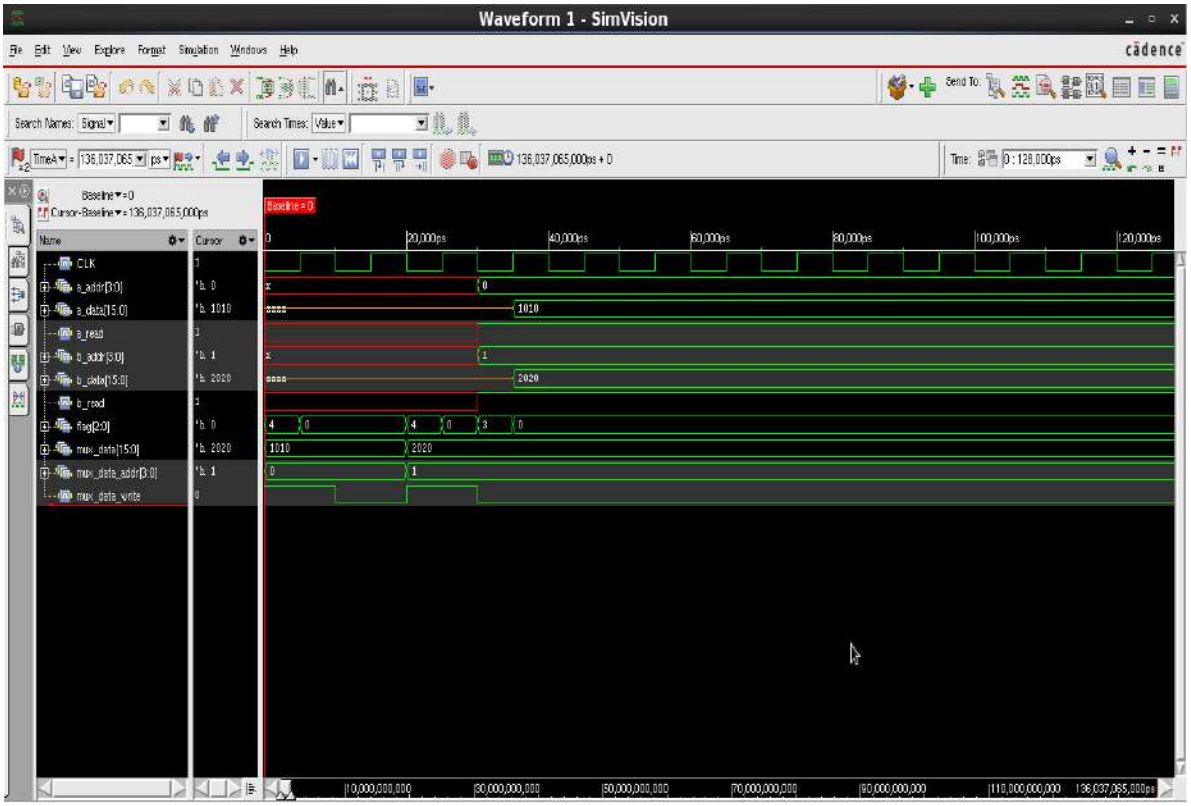

Fig 9: Simulation of REG

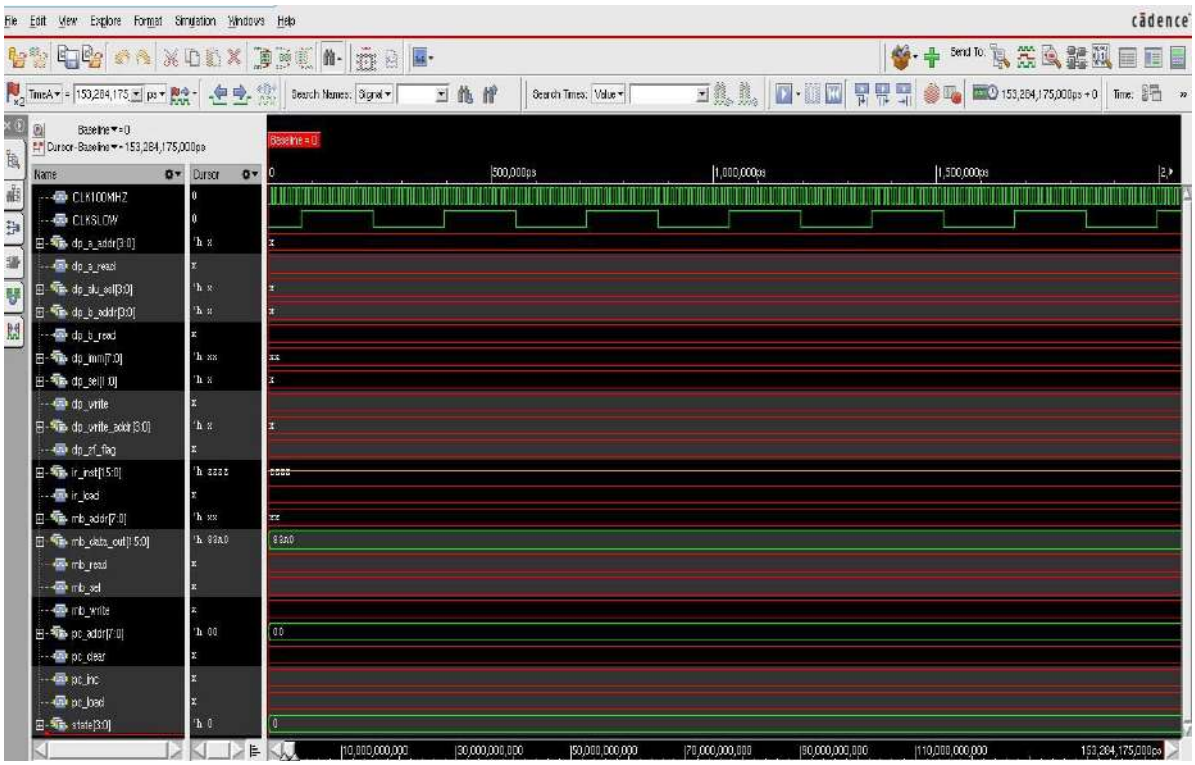

Fig 10: Simulation of cntrl_sim

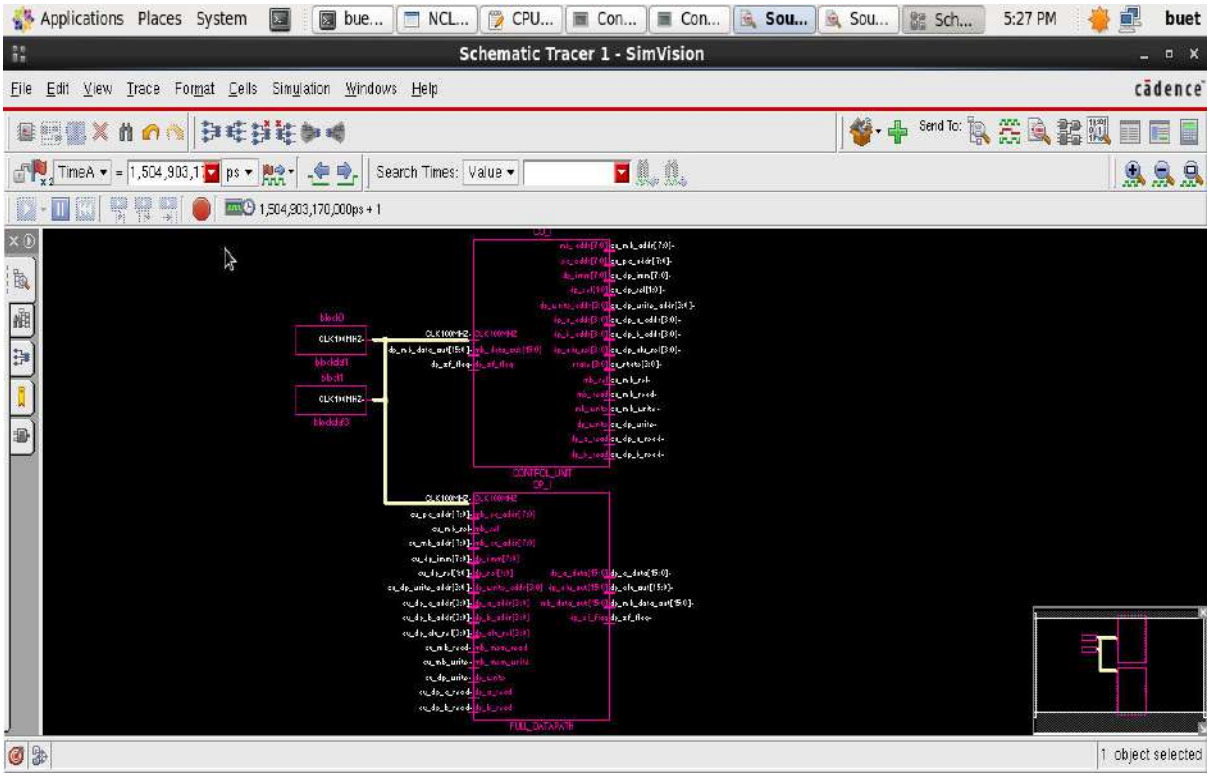

Fig 11: CPU Schematic

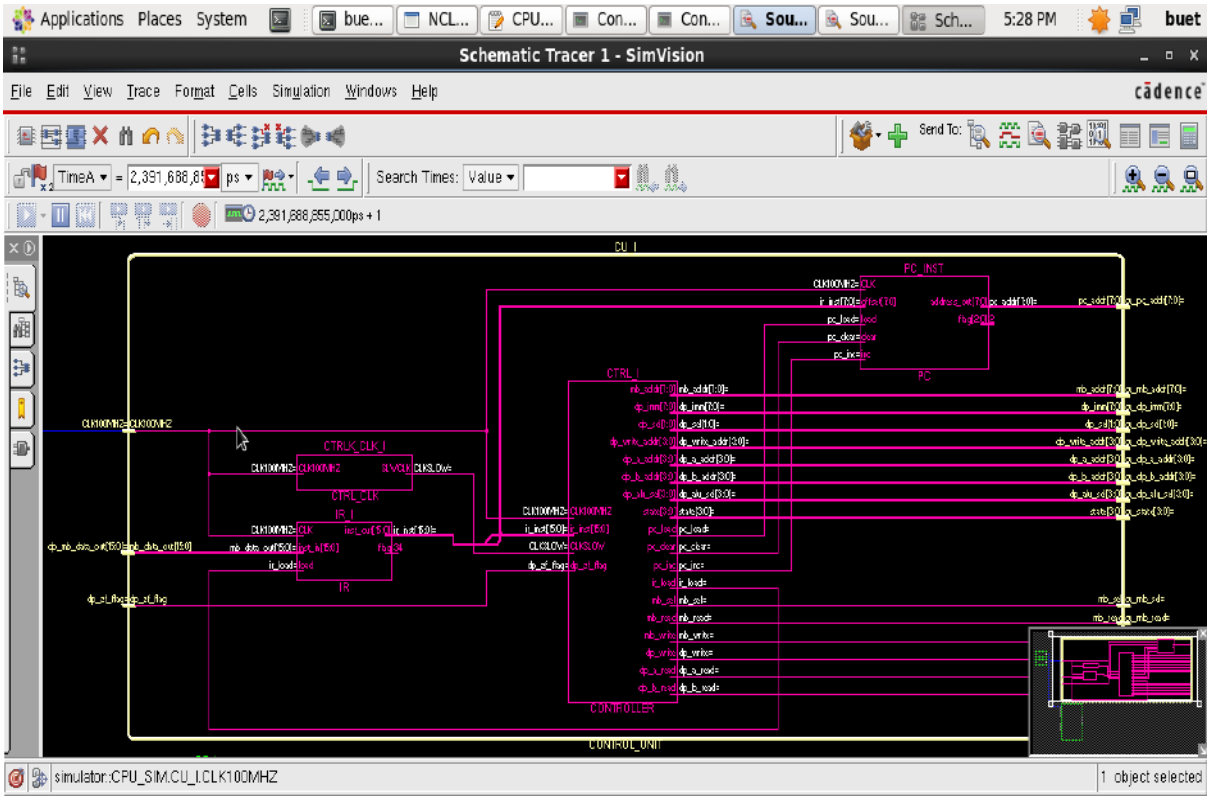

Fig 12: Internal Schematic of CPU

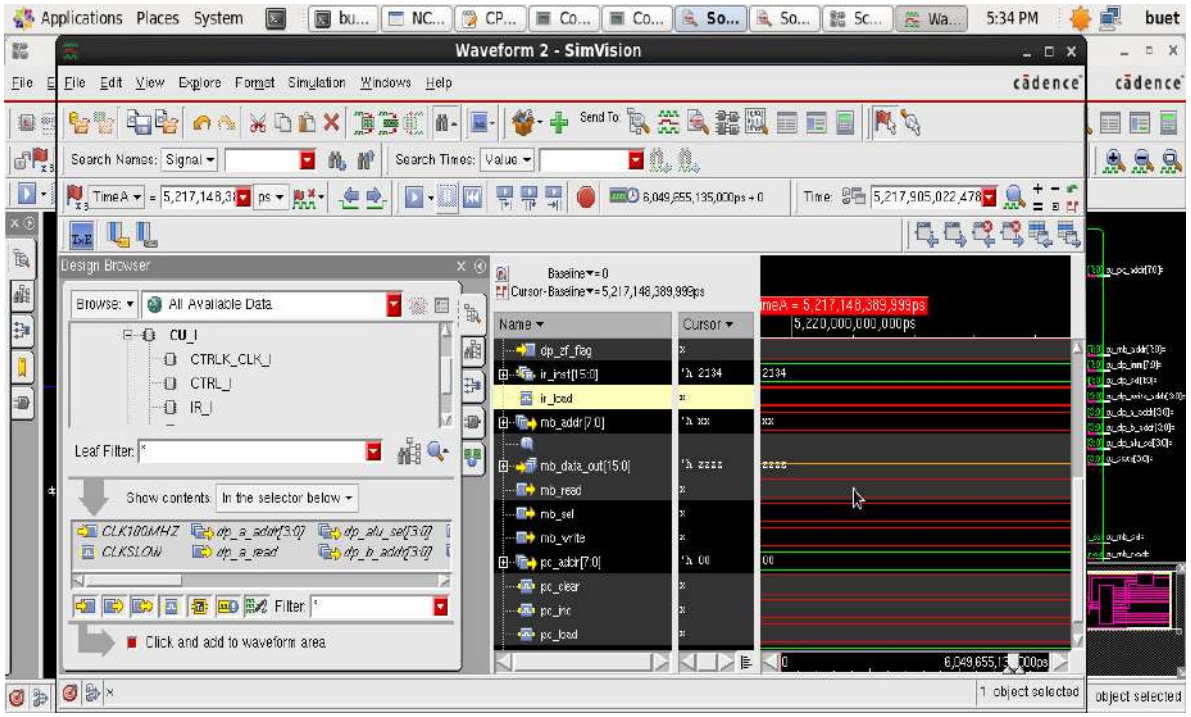

Fig 13: CPU Simulation waveform

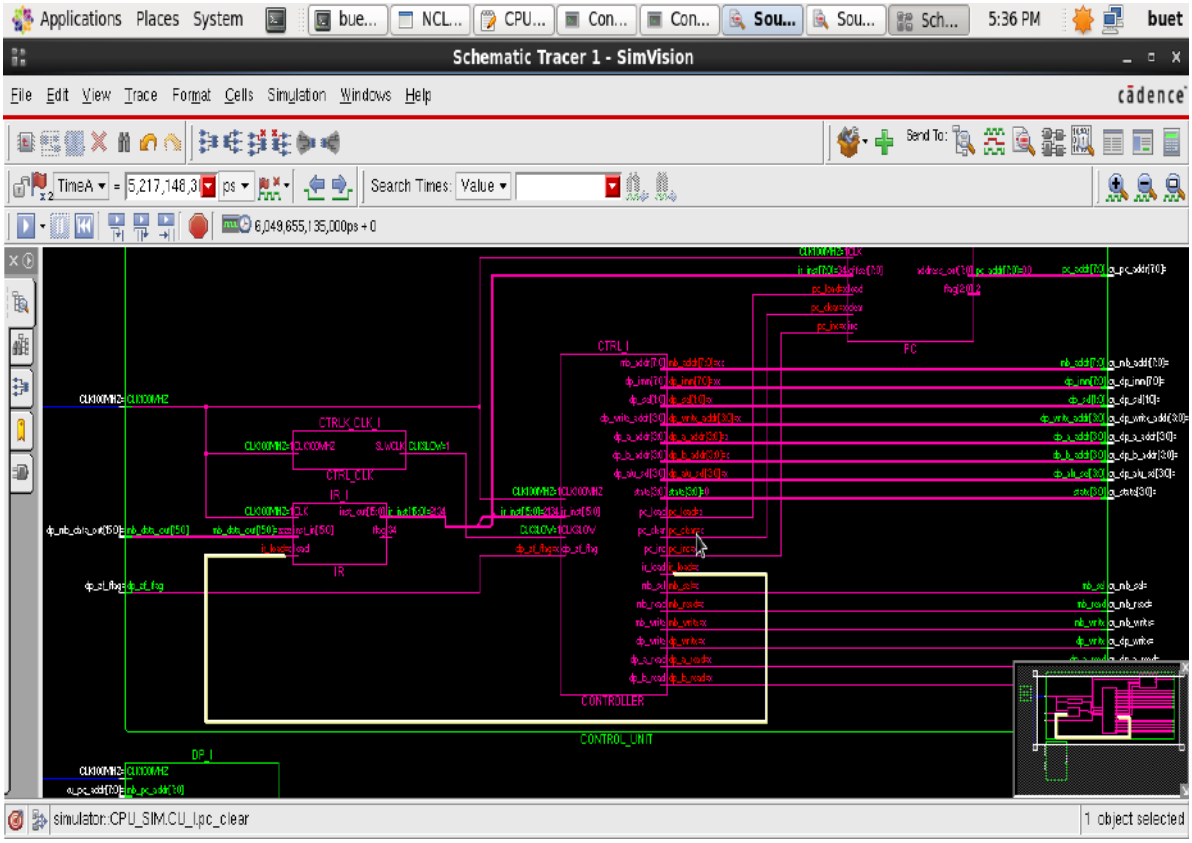

Fig 14: Basic Structure of proposed Design

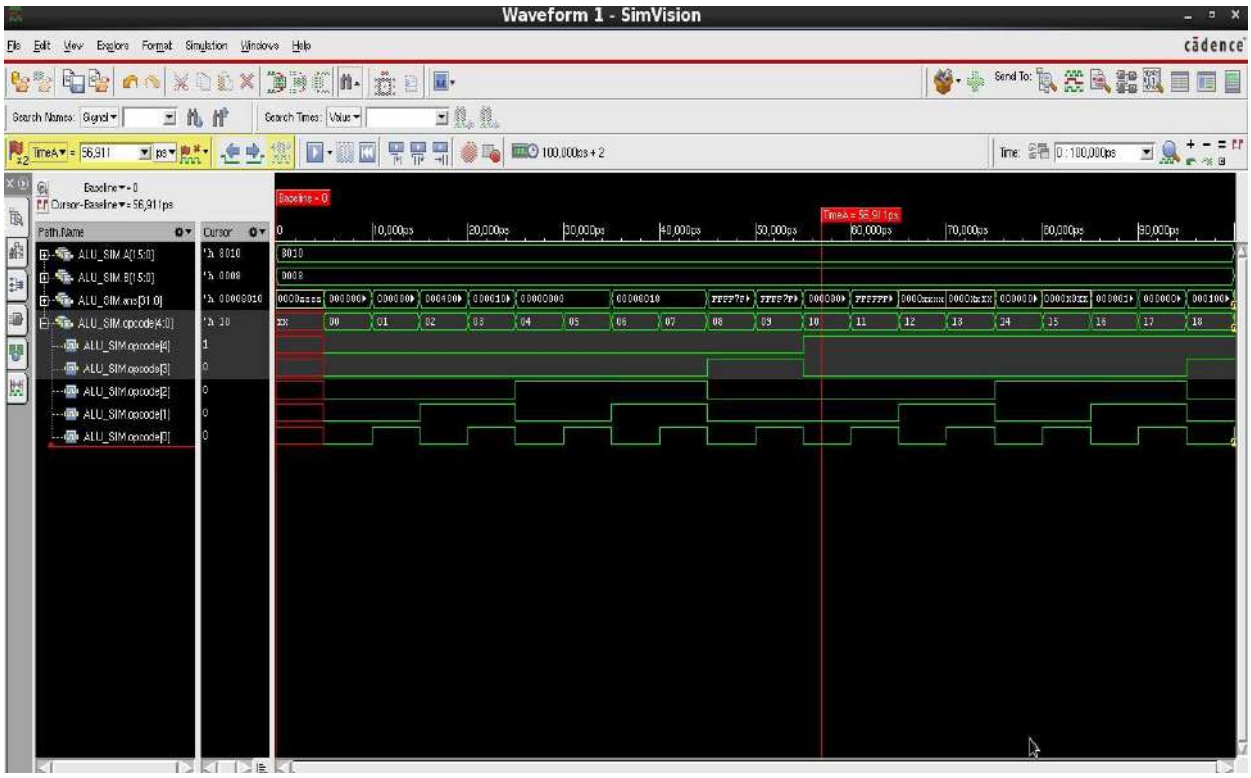

Fig 15: ALU simulation with opcodes

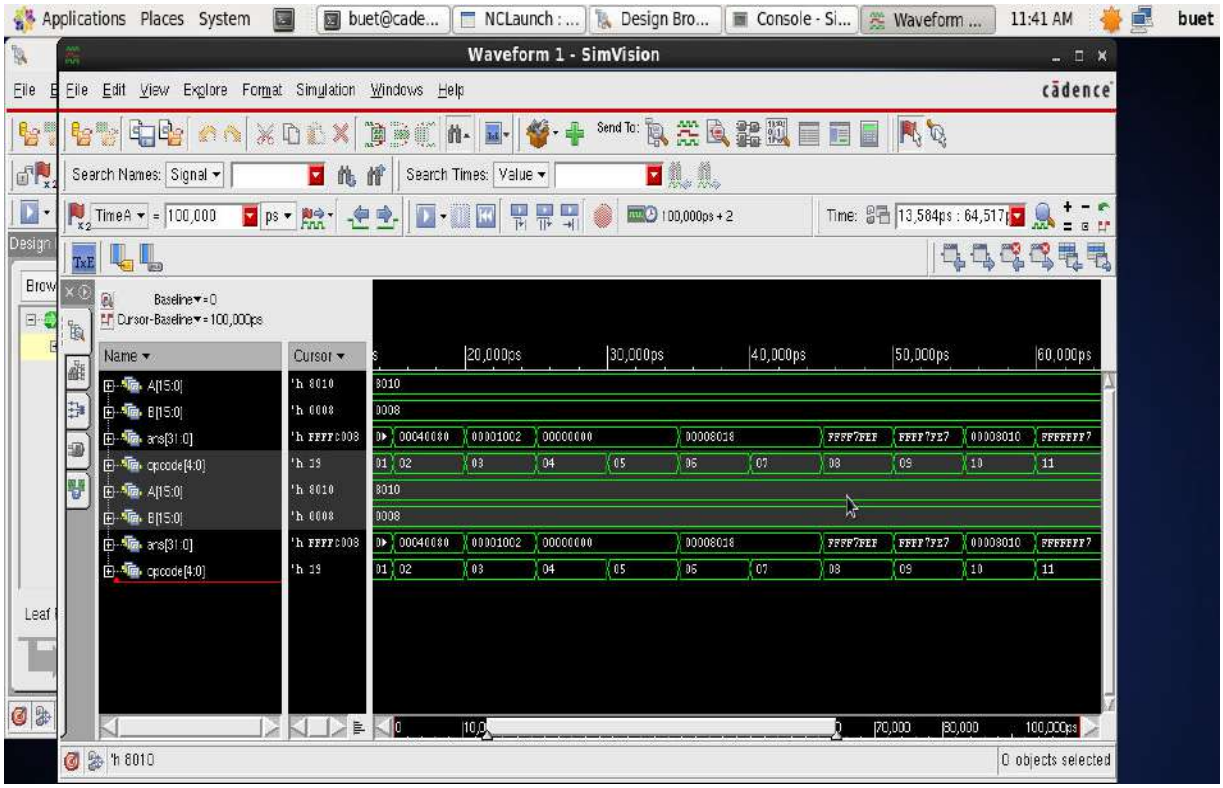

Fig 16: ALU simulation with opcodes with [15:0]A=8010 & [15:0]B=0008

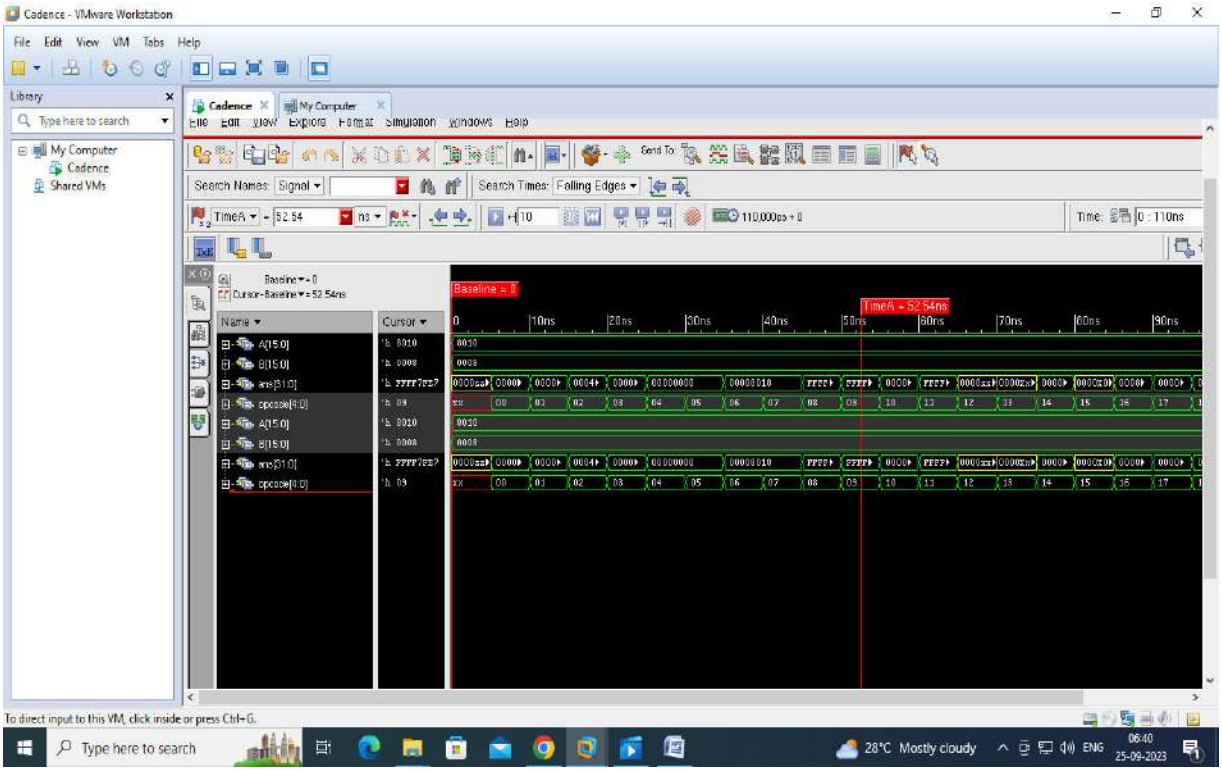

Fig 17: ALU simulation with opcodes with [15:0]A=8010 & [15:0]B=0008 contd…

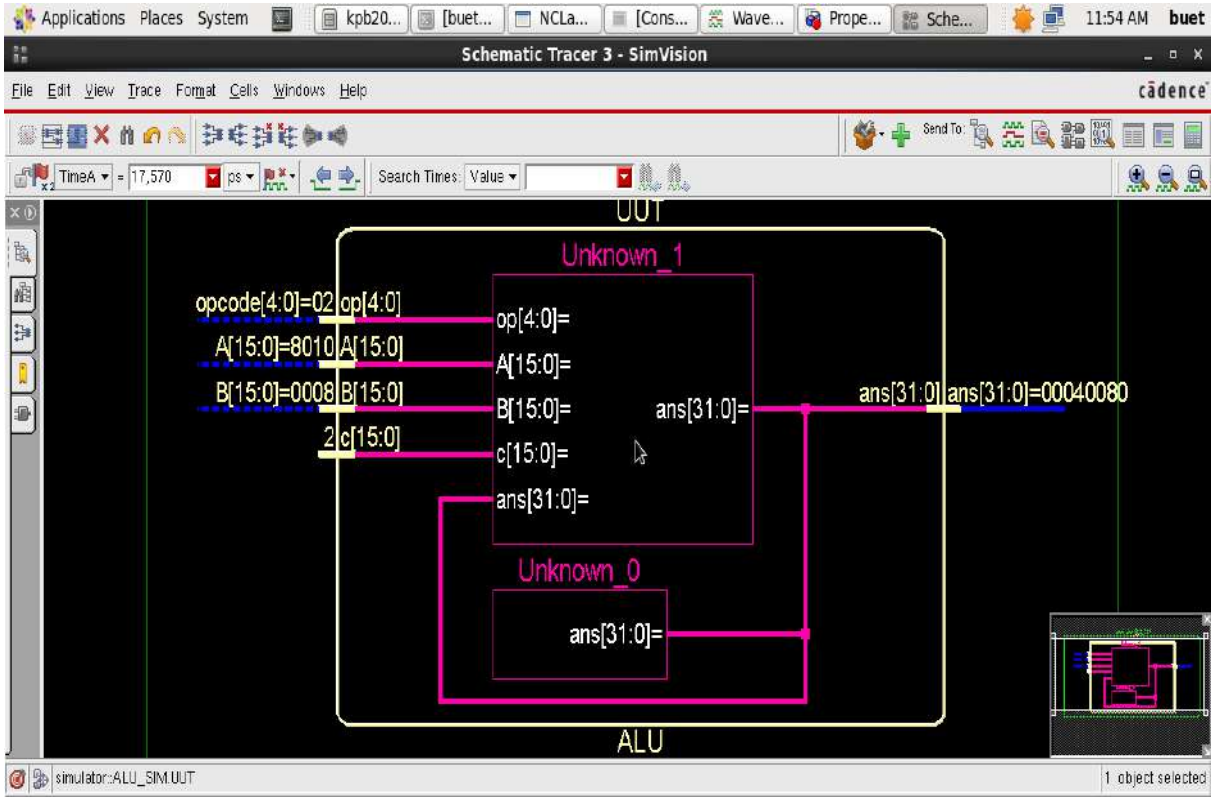

Fig 18: UUT of ALU

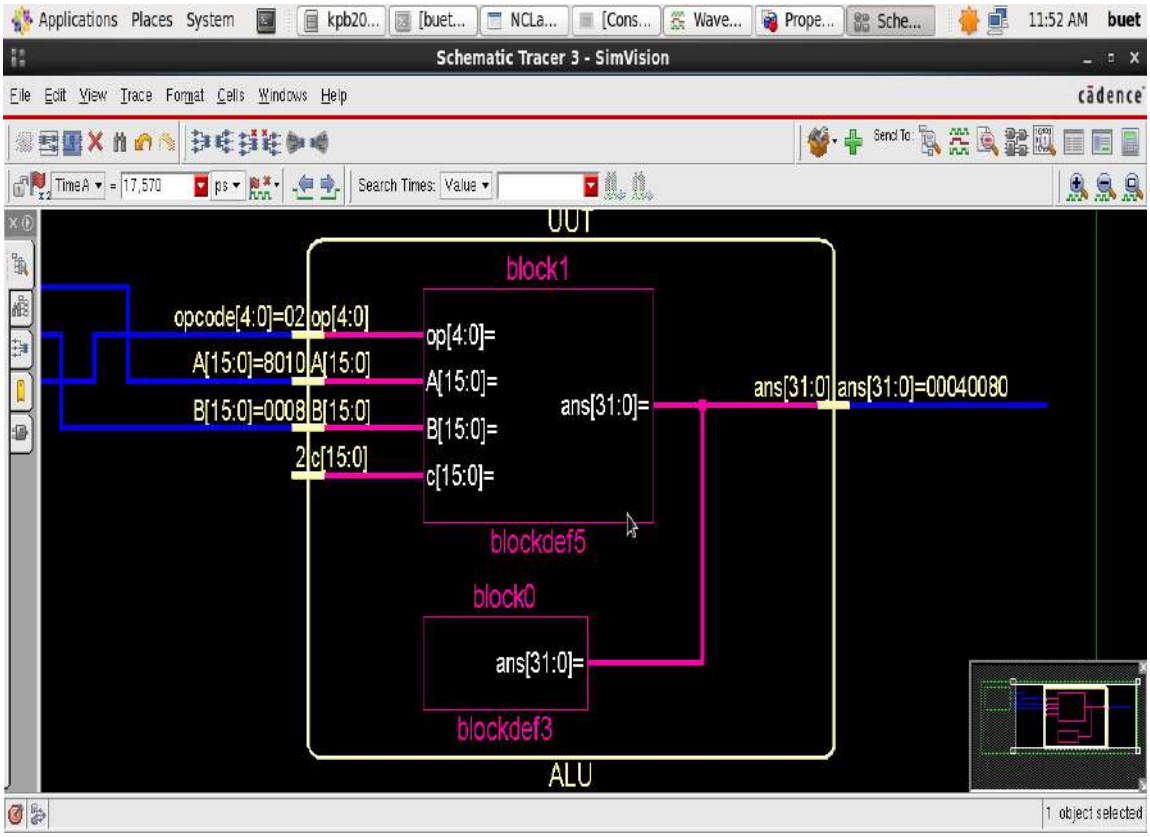

Fig 19: Block UUT of ALU

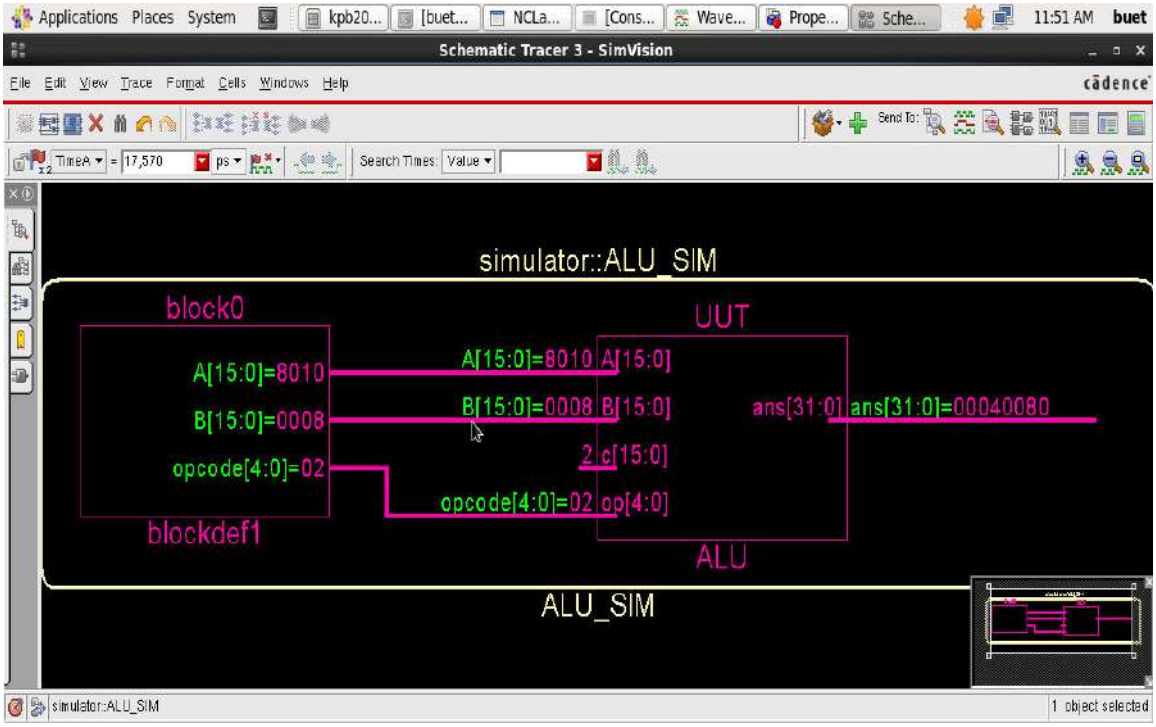

Fig 20: Block Simulator View of ALU

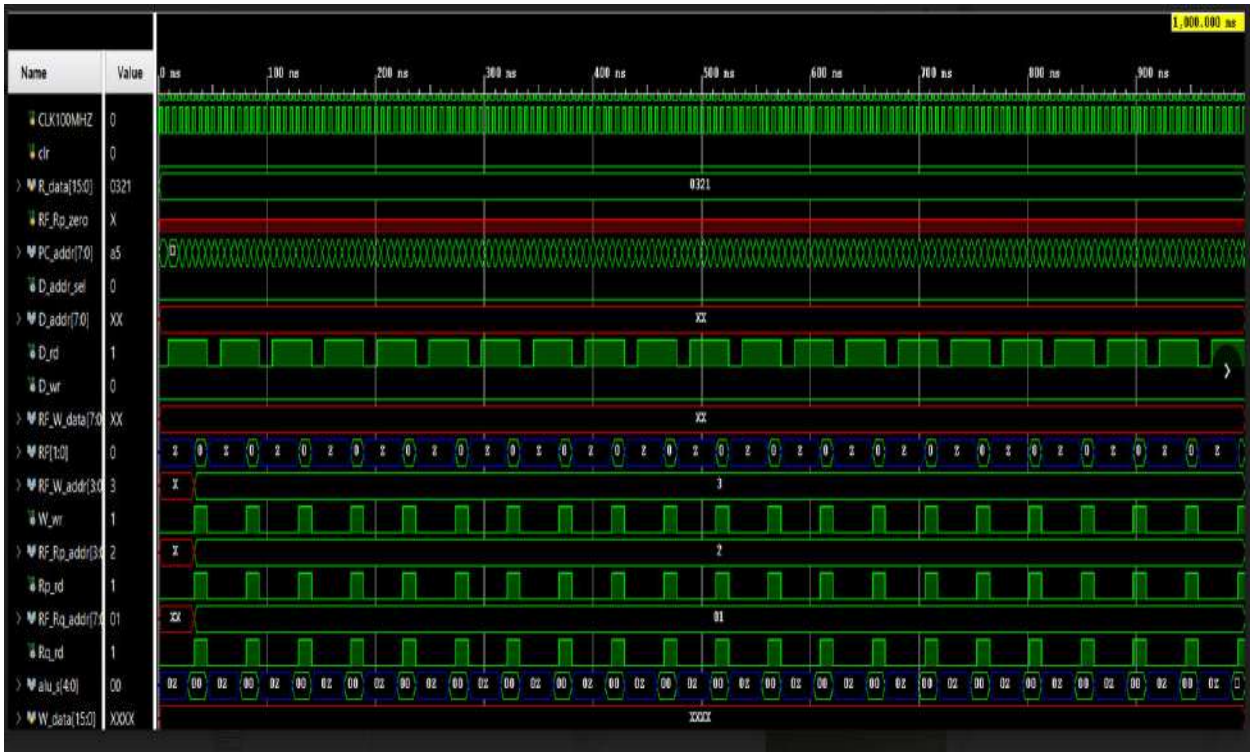

Fig 21: Add Instruction 0x0321 Control Signals From Control Unit

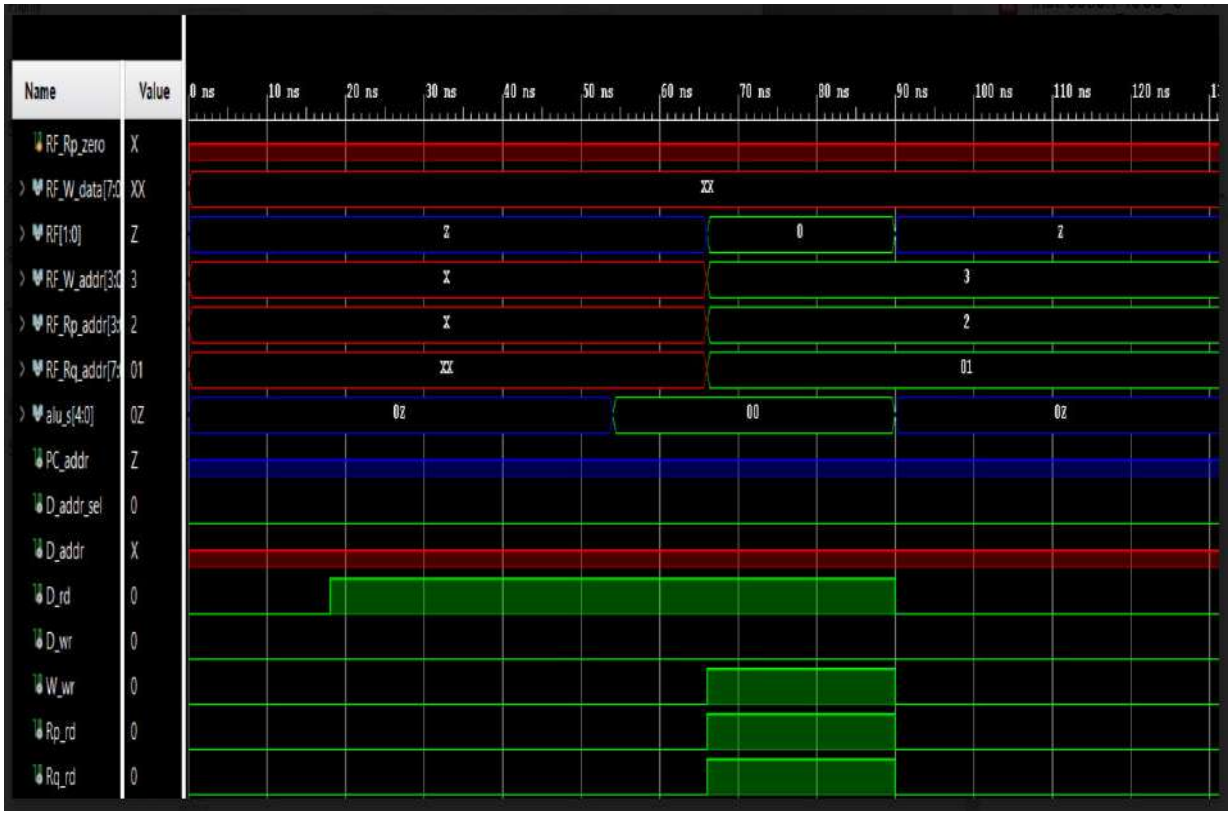

Fig 22: Add Instruction 0x0321 Control Signals From Control

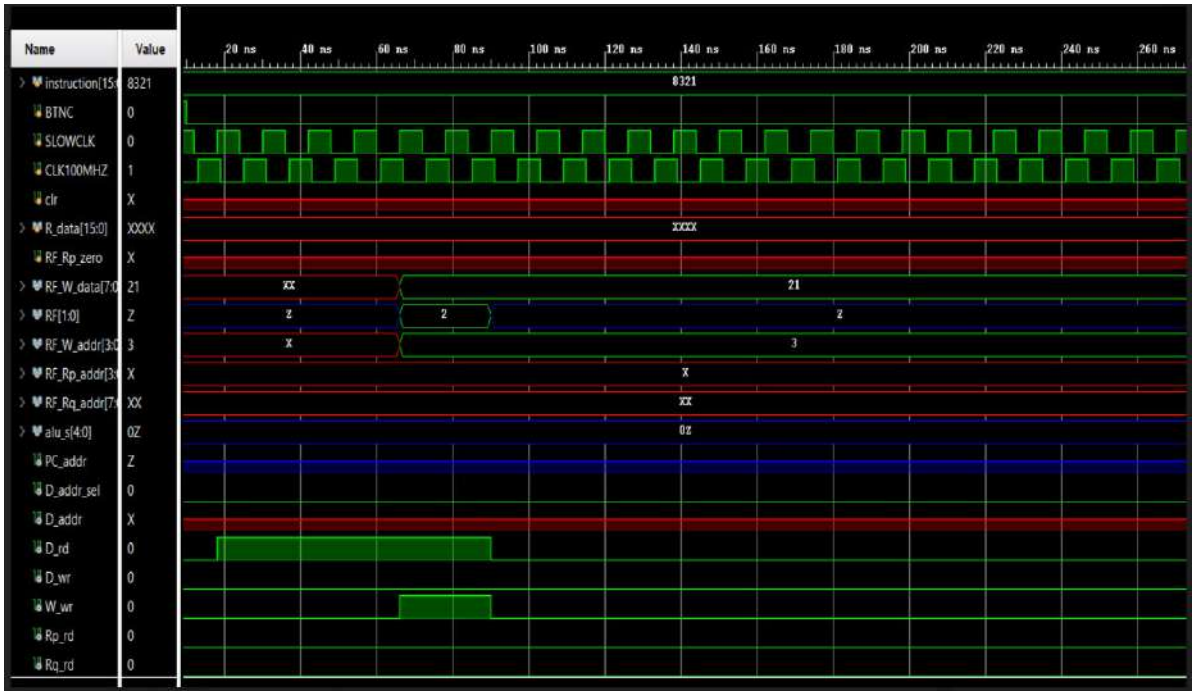

Fig 23: LI Instruction 0x8321 Control Signals From Control Unit

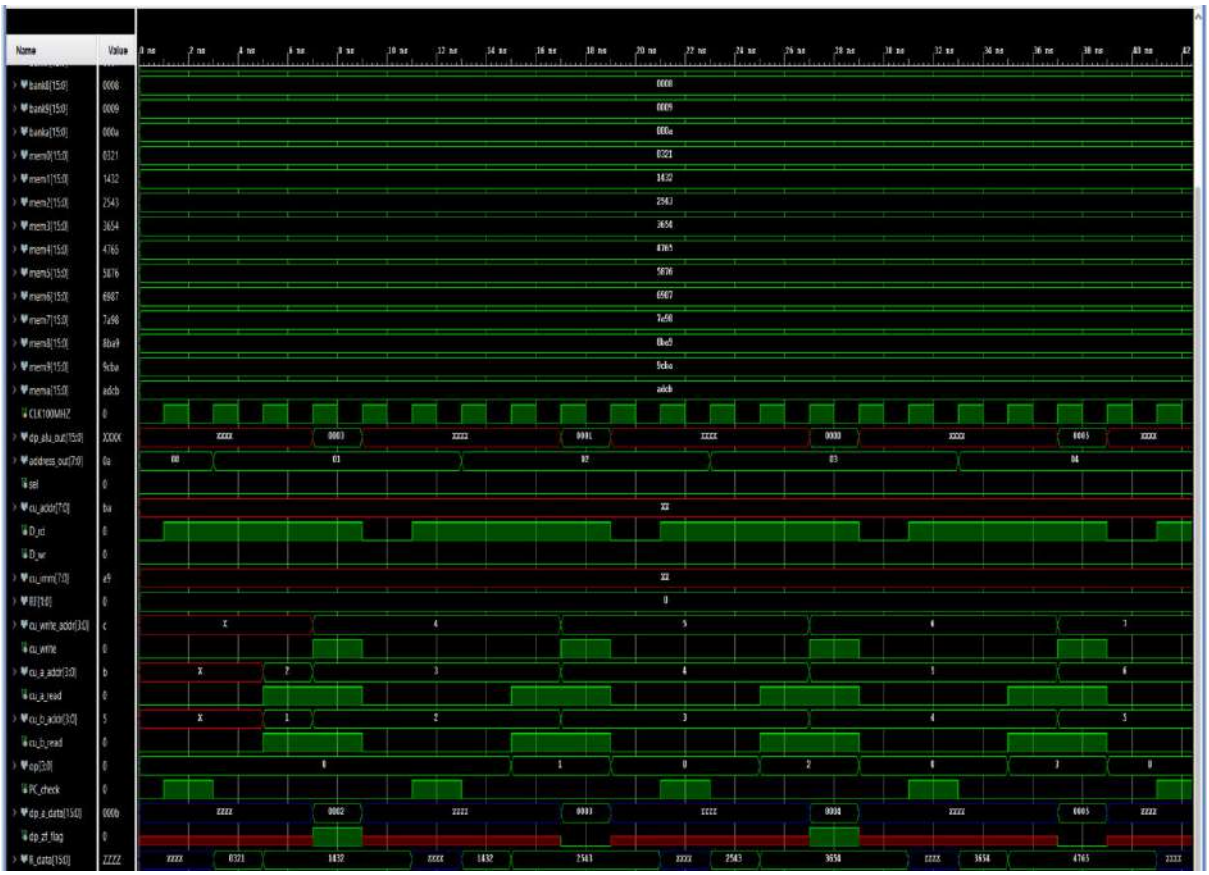

Fig 24: Entire CPU simulation with initial register and memory values

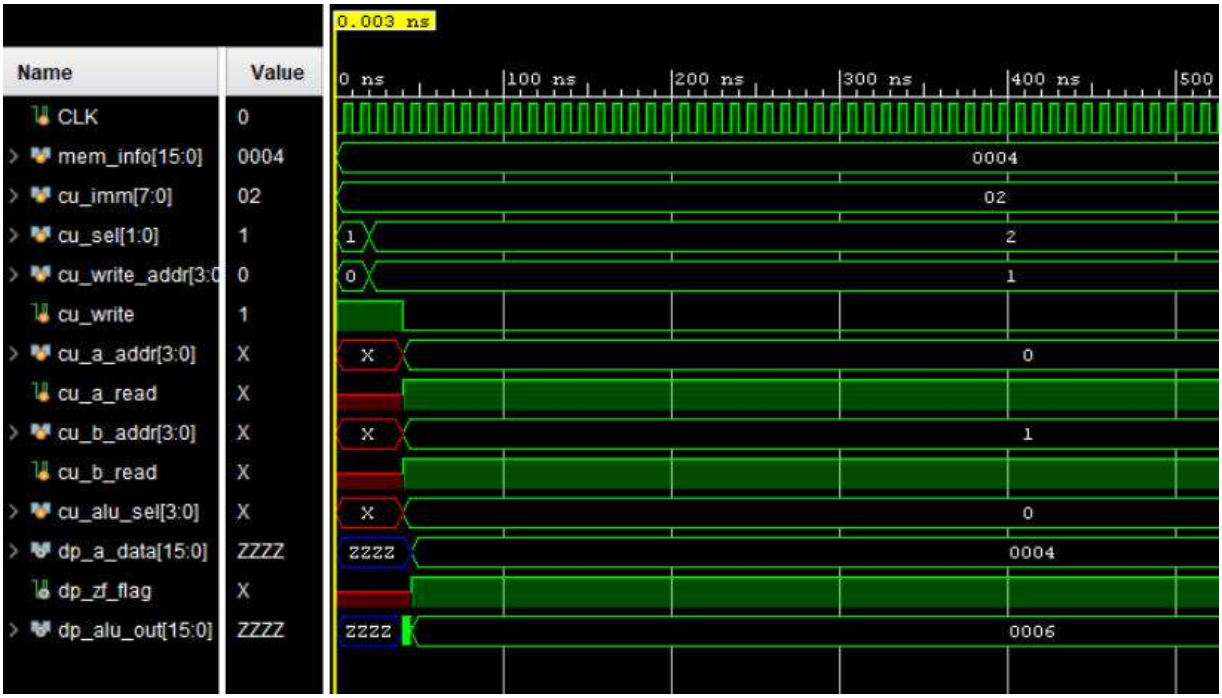

Fig 25: Datapath Simulation

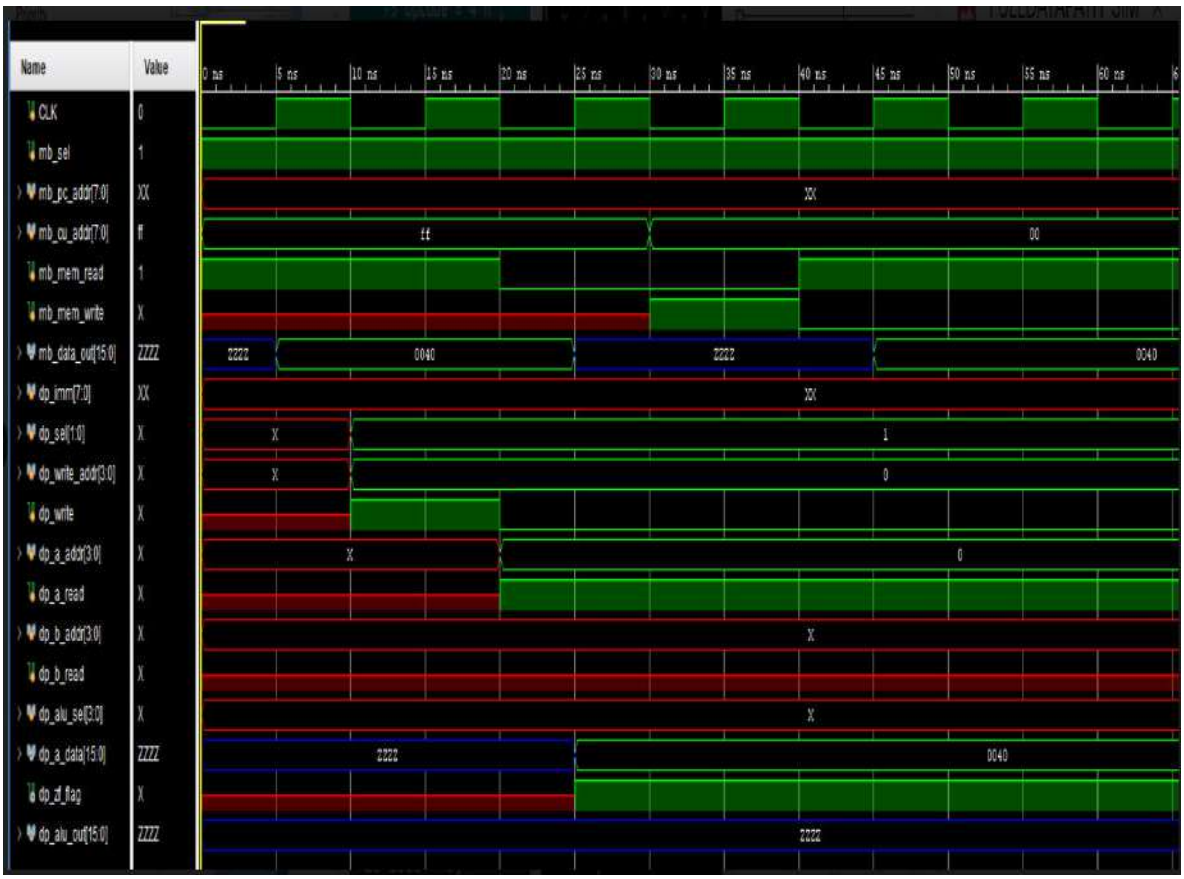

Fig 26: Memory and Datapath Simulation

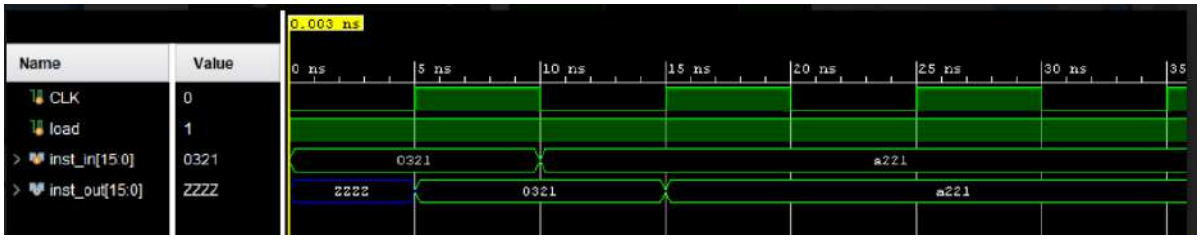

Fig 27: Instruction Register Simulation

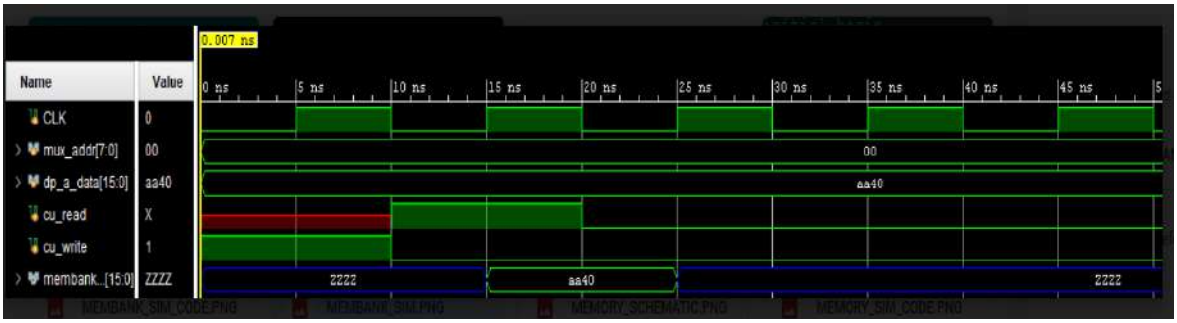

Fig 28: Memory bank Simulation

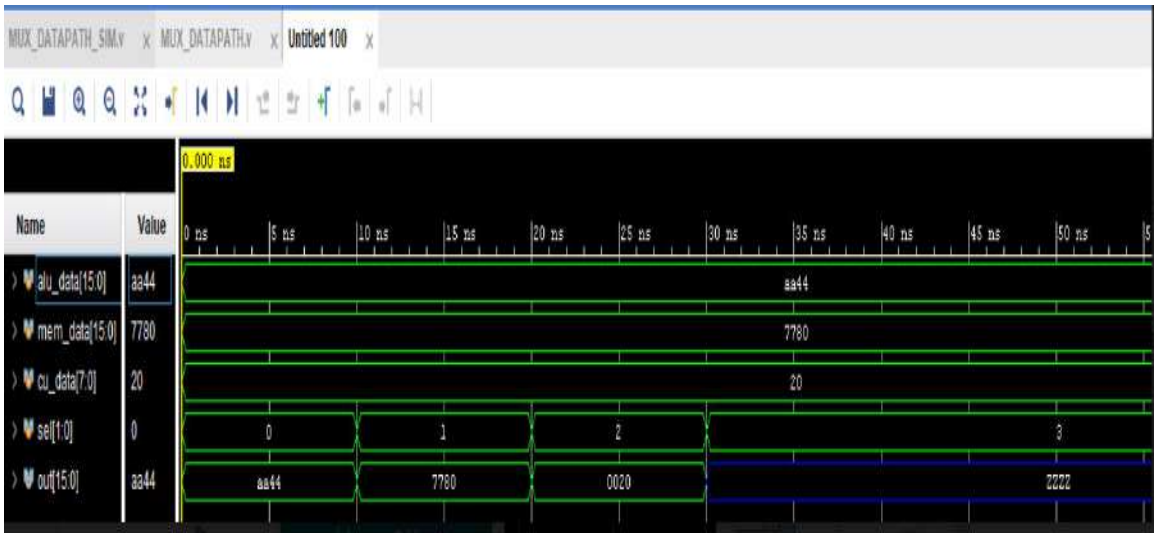

Fig 29: Memory Mux Simulation

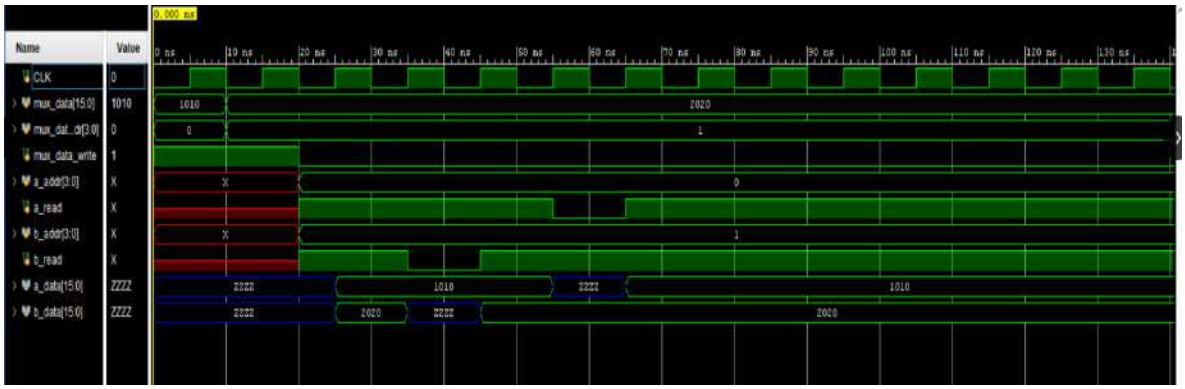

Fig 30: Reg bank Simulation

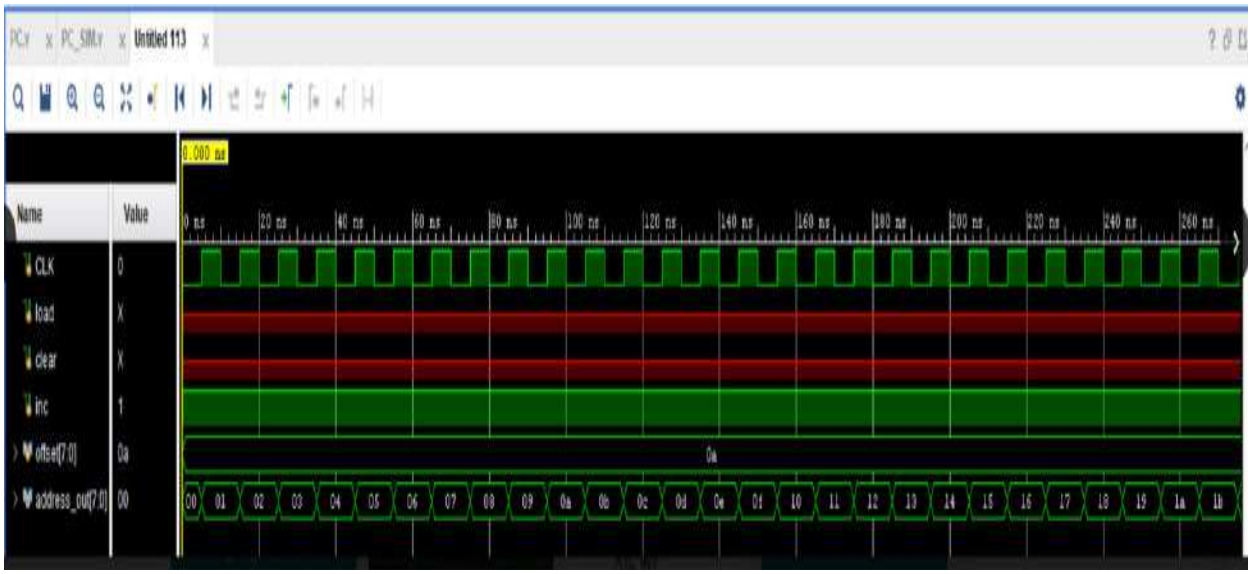

Fig 31: PC Bank Simulation

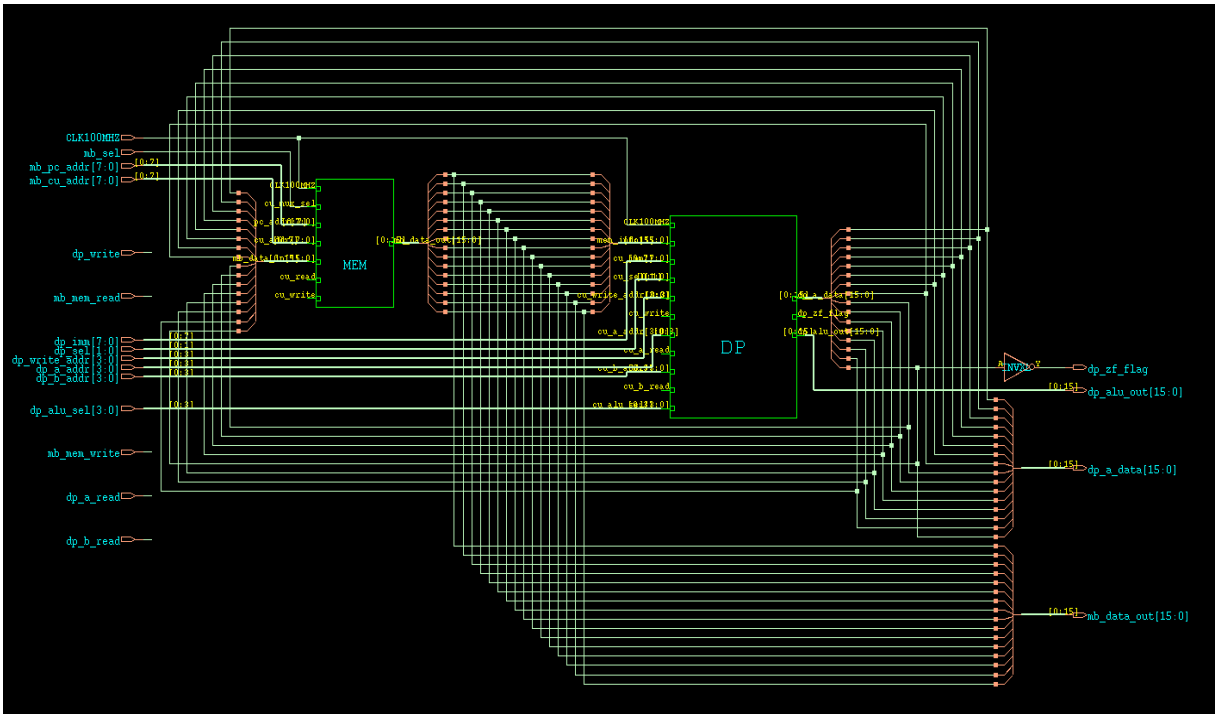

Fig 32: RTL view of Full datapath 45nm.

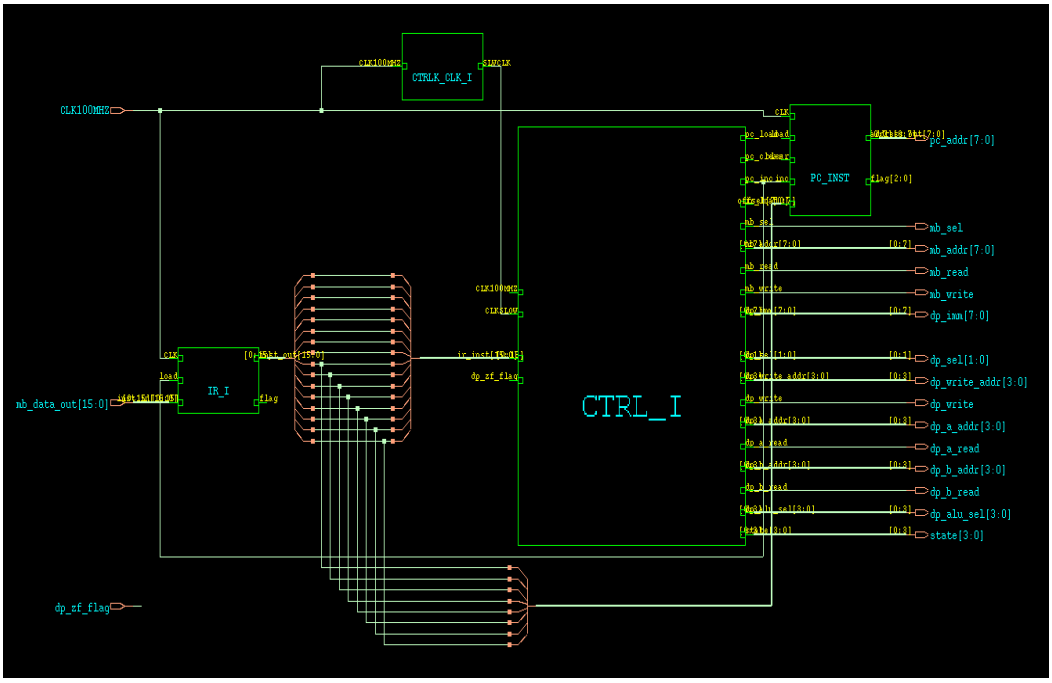

Fig 33: RTL view of Controller 45nm.

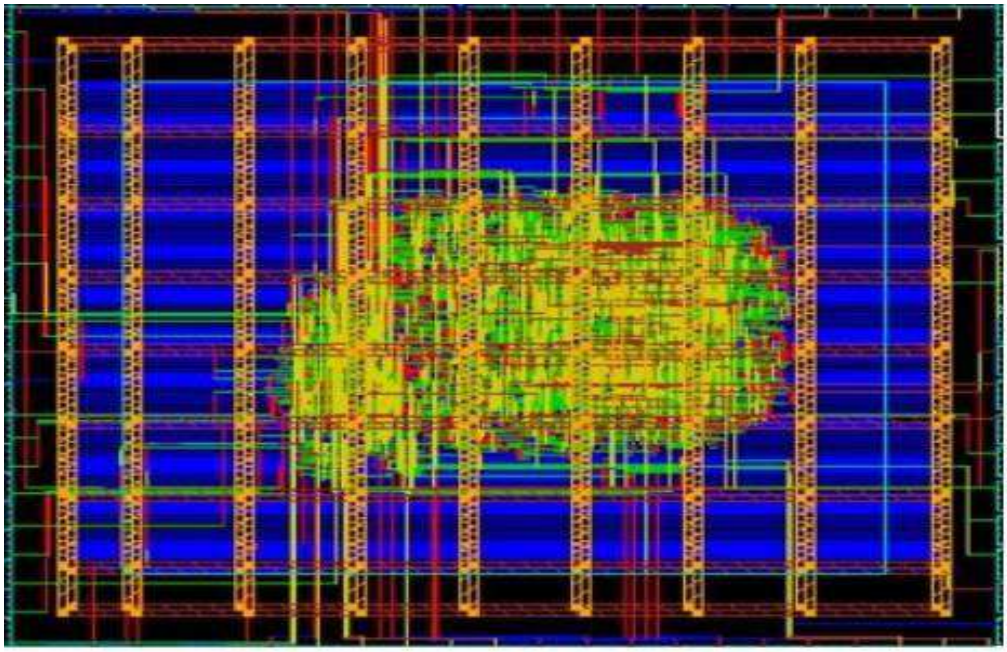

Fig 34: Physical layout

5. CONCLUSION

In this work power optimization technique CDC is used to reduce power consumption by selectively disabling the clock signal to specific parts of the circuit when they are not actively performing computations. This helps conserve power by preventing unnecessary switching activity in idle or non-operational regions of the design. Analyzing clock domain interactions and clock domain crossing issues using Genus is done in this work. Optimization of clock domain architectures to minimize power consumption is encountered successfully.

Comprehensive clock domain crossing analysis to identify and resolve clock domain crossing issues is done. Sequential and combinational optimizations to reduce power consumption using restructuring logic, retiming, and area-based optimization is made in this work. Explicitly insertion of clock gating cells in critical paths where the clock can be gated during inactive periods is compelled in this work.

The full-data-path analysis using 45nm technology are depicted in below figure reports figures 34,35,36,37.

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:23:34 pm
  Module:                 FULL_DATAPATH
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

   Instance      Module     Cell Count  Cell Area  Net Area   Total Area  Wireload
-------------------------------------------------------------------------------------
FULL_DATAPATH                   5925      0.000     0.000        0.000    <none> (D)
  MEM         MEMORY            1669      0.000     0.000        0.000    <none> (D)
    MEMBANK_I MEMBANK           1661      0.000     0.000        0.000    <none> (D)
  DP          DATAPATH          4255      0.000     0.000        0.000    <none> (D)
    REGBANK_I REGBANK           2001      0.000     0.000        0.000    <none> (D)
    MUX_I     MUX_DATAPATH        79      0.000     0.000        0.000    <none> (D)
    ALU_I     ALU               2160      0.000     0.000        0.000    <none> (D)

 (D) = wireload is default in technology library
```

Fig 34: 45nm Genus FD Area report

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:23:34 pm
  Module:                 FULL_DATAPATH
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

                    Leakage      Dynamic       Total
   Instance   Cells Power(nW)    Power(nW)     Power(nW)
-------------------------------------------------------------
FULL_DATAPATH  5925   993.469 739446.27551 739456.21020
  DP           4255   662.042 481444.80093 481451.42136
    REGBANK_I  2001   334.539 355400.23566 355403.58105
    ALU_I      2160   291.989 119137.49490 119140.41478
    MUX_I        79    30.014   1593.39888   1593.69902
  MEM          1669   331.407 222752.96427 222756.27834
    MEMBANK_I  1661   329.657 222727.46105 222730.75762
```

Fig 35: 45nm Genus FD power report

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023   12:23:34 pm
  Module:                 FULL_DATAPATH
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: VIOLATED (-877 ps) Setup Check with Pin MEM/MEMBANK_I/data_out_reg[0]/CK->D
          Group: CLK100MHZ
     Startpoint: (R) DP/REGBANK_I/a_data_reg[0]/CK
          Clock: (R) CLK100MHZ
       Endpoint: (F) MEM/MEMBANK_I/data_out_reg[0]/D
          Clock: (R) CLK100MHZ

                    Capture       Launch
       Clock Edge:+     100            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=    100            0

             Setup:-     -17
       Uncertainty:-      10
     Required Time:=     107
      Launch Clock:-       0
         Data Path:-     983
             Slack:=    -877


#-------------------------------------------------------------------------------------------------------
#          Timing Point          Flags   Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                               (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------
  DP/REGBANK_I/a_data_reg[0]/CK   -       -     R     (arrival)    517    -   100     -       0    (-,-)
  DP/REGBANK_I/a_data_reg[0]/Q    -       CK->Q F     DFFHQX8       10 20.1    62   322     322    (-,-)
  MEM/MEMBANK_I/fopt284262/Y      -       A->Y  R     CLKINVX4       3  8.6    45    44     366    (-,-)
  MEM/MEMBANK_I/fopt284281/Y      -       A->Y  F     INVX6          8  7.2    32    34     400    (-,-)
  MEM/MEMBANK_I/g152546/Y         -       A->Y  R     MXI2X1         1  0.9    73    59     460    (-,-)
  MEM/MEMBANK_I/g152076/Y         -       B->Y  F     NOR2X1         1  1.5    46    49     508    (-,-)
  MEM/MEMBANK_I/g151932/Y         -       B0->Y R     AOI21X2        1  1.7    58    46     555    (-,-)
  MEM/MEMBANK_I/g151833/Y         -       A->Y  F     NAND2X2        1  1.6    58    59     614    (-,-)
  MEM/MEMBANK_I/g151780/Y         -       A0->Y R     OAI21X2        1  2.9    84    74     688    (-,-)
  MEM/MEMBANK_I/g151763/Y         -       B0->Y F     OAI21X4        1  1.7    58    65     753    (-,-)
  MEM/MEMBANK_I/g151746/Y         -       A->Y  R     NOR2X2         1  1.6    52    54     807    (-,-)
  MEM/MEMBANK_I/g151739/Y         -       A0->Y F     AOI21X2        1  1.5    69    70     877    (-,-)
  MEM/MEMBANK_I/g151737/Y         -       B0->Y R     AOI21X2        1  1.7    58    54     931    (-,-)
  MEM/MEMBANK_I/g151736/Y         -       A->Y  F     NAND2X2        1  0.8    46    53     983    (-,-)
  MEM/MEMBANK_I/data_out_reg[0]/D <<<     -     F     DFFHQX4        1    -     -     0      983    (-,-)
#-------------------------------------------------------------------------------------------------------
```

Fig 36: 45nm Genus FD timing report

```
╞=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:23:34 pm
  Module:                 FULL_DATAPATH
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================
```

Gate	Instances	Area	Library
ACHCONX2	93	0.000	slow
ADDFX4	1	0.000	slow
ADDFXL	275	0.000	slow
ADDHX1	3	0.000	slow
AND2X6	1	0.000	slow
AND2X8	5	0.000	slow
AND3X1	4	0.000	slow
AND3X2	3	0.000	slow
AND4XL	2	0.000	slow
AO21X1	48	0.000	slow
AO21X2	35	0.000	slow
AO22X1	19	0.000	slow
AO22X2	31	0.000	slow
AO22XL	74	0.000	slow
AOI211XL	22	0.000	slow
AOI21X1	56	0.000	slow
AOI21X2	225	0.000	slow
AOI21X4	180	0.000	slow
AOI221X1	4	0.000	slow
AOI221XL	80	0.000	slow
AOI222X1	1	0.000	slow
AOI222X2	3	0.000	slow
AOI222XL	7	0.000	slow
AOI211XL	22	0.000	slow
AOI21X1	56	0.000	slow
AOI21X2	225	0.000	slow
AOI21X4	180	0.000	slow
AOI221X1	4	0.000	slow
AOI221XL	80	0.000	slow
AOI222X1	1	0.000	slow
AOI222X2	3	0.000	slow
AOI222XL	7	0.000	slow
AOI22X1	80	0.000	slow
AOI22X2	2	0.000	slow
AOI22X4	2	0.000	slow
AOI2BB1X2	1	0.000	slow
AOI2BB1X4	9	0.000	slow
AOI31XL	6	0.000	slow
AOI32XL	6	0.000	slow
AOI33XL	1	0.000	slow
BUFX12	2	0.000	slow
BUFX16	3	0.000	slow
BUFX6	1	0.000	slow
CLKAND2X12	14	0.000	slow
CLKINVX1	448	0.000	slow
CLKINVX12	5	0.000	slow
CLKINVX16	10	0.000	slow
CLKINVX2	517	0.000	slow
CLKINVX20	12	0.000	slow
CLKINVX3	78	0.000	slow
CLKINVX4	106	0.000	slow
CLKINVX6	1	0.000	slow
CLKINVX8	53	0.000	slow
CLKMX2X3	7	0.000	slow
CLKMX2X8	1	0.000	slow
DFFHQX1	199	0.000	slow
DFFHQX4	23	0.000	slow
DFFHQX8	1	0.000	slow
DFFX1	4	0.000	slow

```
OR3X1                13  0.000     slow
OR3X2                 2  0.000     slow
OR4X1                 6  0.000     slow
OR4XL                 3  0.000     slow
TBUFX20              16  0.000     slow
TLATX4               16  0.000     slow
XNOR2X1              27  0.000     slow
XNOR2X2              71  0.000     slow
XNOR2X4               2  0.000     slow
XNOR3X1              70  0.000     slow
XOR2X4               10  0.000     slow
XOR3XL               26  0.000     slow
---------------------------------------
total              5925  0.000


     Type       Instances  Area Area %
---------------------------------------
sequential            533 0.000    0.0
inverter             1313 0.000    0.0
buffer                 21 0.000    0.0
tristate               16 0.000    0.0
logic                4042 0.000    0.0
physical_cells          0 0.000    0.0
---------------------------------------
total                5925 0.000    0.0
```

Fig 37: 45nm Genus FD Gate count report

The Controller analysis using 45nm technology are depicted in below reports figures 38,39,40,41.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:16:06 pm
  Module:                 CONTROL_UNIT
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

   Instance     Module    Cell Count  Cell Area  Net Area   Total Area  Wireload
-------------------------------------------------------------------------------------
CONTROL_UNIT                   221      0.000     0.000        0.000    <none> (D)
  PC_INST     PC                96      0.000     0.000        0.000    <none> (D)
  CTRL_I      CONTROLLER       107      0.000     0.000        0.000    <none> (D)
  CTRLK_CLK_I CTRL_CLK          18      0.000     0.000        0.000    <none> (D)

 (D) = wireload is default in technology library
```

Fig 38: 45nm Genus Controller Area report

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:16:06 pm
  Module:                 CONTROL_UNIT
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                    Leakage    Dynamic      Total
   Instance   Cells Power(nW)  Power(nW)   Power(nW)
-----------------------------------------------------------
CONTROL_UNIT    221    47.615 201620.4980 201625.2594
  CTRL_I        107    23.446  16865.5586  16867.9032
  PC_INST        96    19.918 109011.3212 109013.3130
  CTRLK_CLK_I    18     4.250  60858.1964  60858.6214
  IR_I            0     0.000   5787.5011   5787.5011
```

Fig 39: 45nm Genus Controller total power report

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1
  Generated on:           Nov 21 2023  12:16:06 pm
  Module:                 CONTROL_UNIT
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: VIOLATED (-438 ps) Setup Check with Pin CTRLK_CLK_I/SLWCLK_reg/CK->SI
           Group: CLK100MHZ
      Startpoint: (R) CTRLK_CLK_I/CTR_reg[3]/CK
           Clock: (R) CLK100MHZ
        Endpoint: (R) CTRLK_CLK_I/SLWCLK_reg/SI
           Clock: (R) CLK100MHZ

                     Capture       Launch
       Clock Edge:+      100            0
      Src Latency:+        0            0
      Net Latency:+        0 (I)        0 (I)
          Arrival:=      100            0

            Setup:-      137
      Uncertainty:-       10
     Required Time:=      -47
      Launch Clock:-        0
         Data Path:-      392
             Slack:=     -438
```

Timing Point	Flags	Arc	Edge	Cell	Fanout	Load (fF)	Trans (ps)	Delay (ps)	Arrival (ps)	Instance Location
CTRLK_CLK_I/CTR_reg[3]/CK	-	-	R	(arrival)	14	-	100	-	0	(-,-)
CTRLK_CLK_I/CTR_reg[3]/Q	-	CK->Q	F	DFFQX4	1	4.2	36	290	290	(-,-)
CTRLK_CLK_I/fopt845/Y	-	A->Y	R	INVX6	2	6.7	28	28	318	(-,-)
CTRLK_CLK_I/g832__4547/Y	-	B->Y	F	NAND2X8	2	3.6	48	38	356	(-,-)
CTRLK_CLK_I/g827__4296/Y	-	B->Y	R	NOR2X4	2	1.4	39	36	392	(-,-)
CTRLK_CLK_I/SLWCLK_reg/SI	<<<	-	R	SDFFHQX4	2	-	-	0	392	(-,-)

Fig 40: 45nm Genus Controller Timing report

Generated by:	Genus(TM) Synthesis Solution 17.22-s017_1
Generated on:	Nov 21 2023 12:16:06 pm
Module:	CONTROL_UNIT
Technology library:	slow
Operating conditions:	slow (balanced_tree)
Wireload mode:	enclosed
Area mode:	timing library

Gate	Instances	Area	Library
ADDFXL	3	0.000	slow
ADDHX2	4	0.000	slow
AND3X1	2	0.000	slow
AND3XL	1	0.000	slow
AO21X1	8	0.000	slow
AO22X1	6	0.000	slow
AO22XL	1	0.000	slow
AOI222XL	1	0.000	slow
AOI22XL	1	0.000	slow
BUFX20	3	0.000	slow
CLKAND2X12	1	0.000	slow
CLKINVX1	14	0.000	slow
CLKINVX16	1	0.000	slow
CLKINVX2	2	0.000	slow
CLKINVX4	26	0.000	slow
CLKINVX8	2	0.000	slow
CLKMX2X12	4	0.000	slow
DFFHQX4	9	0.000	slow
DFFQX4	2	0.000	slow
DFFX4	4	0.000	slow
INVX2	1	0.000	slow
INVX4	1	0.000	slow
INVX6	1	0.000	slow
INVX2	1	0.000	slow
INVX4	1	0.000	slow
INVX6	1	0.000	slow
INVXL	1	0.000	slow
MXI2X1	1	0.000	slow
NAND2BX1	1	0.000	slow
NAND2BX4	1	0.000	slow
NAND2BXL	4	0.000	slow
NAND2X4	1	0.000	slow
NAND2X8	2	0.000	slow
NAND3BXL	3	0.000	slow
NAND3X1	1	0.000	slow
NAND4BX4	1	0.000	slow
NOR2BXL	16	0.000	slow
NOR2X4	1	0.000	slow
NOR2X8	2	0.000	slow
OA21X1	3	0.000	slow
OA21X2	1	0.000	slow
OAI21X4	8	0.000	slow
OAI21XL	1	0.000	slow
OAI221XL	1	0.000	slow
OAI31XL	1	0.000	slow
OAI32XL	1	0.000	slow
OR2X1	9	0.000	slow

OR2X2	1	0.000	slow
OR2X8	3	0.000	slow
OR2XL	2	0.000	slow
OR3X1	3	0.000	slow
SDFFHQX4	2	0.000	slow
TLATNX2	41	0.000	slow
TLATX4	4	0.000	slow
XNOR2X1	2	0.000	slow
XNOR2X2	2	0.000	slow
XNOR3X1	1	0.000	slow
XOR2X4	2	0.000	slow
total	221	0.000	

Type	Instances	Area	Area %
sequential	62	0.000	0.0
inverter	49	0.000	0.0
buffer	3	0.000	0.0
logic_abstract	1	0.000	0.0
logic	107	0.000	0.0
physical_cells	0	0.000	0.0
total	222	0.000	0.0

Fig 41: 45nm Genus Controller gate count report

6. CONCLUSION

The results in [9] has got the power value of 10.5mw, in [10] they got 1.72 mw power dissipation value, in [11], the authors mentioned the power value as 1.1649 mw. In [12], the authors got the power value as 17.85372661mw.The proposed work got the power report as 0.73945621020mw for FD with no of cells as 5925 and 0.2016252594mw for controller with no of cells as 222, which are optimum results when compared with them[9,10,11,12].

7. FUTURE-SCOPE

By integrating clock gating, power gating into the RISC processor design using Cadence tools, designers can achieve significant power savings during periods of inactivity, contributing to overall energy efficiency in embedded systems.

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