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EFFICIENT LOW-POWER 8T SRAM DESIGN WITH SCHMITT TRIGGER LOGIC

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ABSTRACT
An 8-transistor SRAM cell (ST) can have its power consumption reduced, according to this study, by employing Schmitt Trigger logic. In this work, we will examine the architecture of SRAM cells with the main objective of improving the reliability of SRAM access while decreasing power consumption. The design is shown here after it has been simulated using 0.18 nm process technologies. With its bit interleaving structure, which does not have write backs, the 9-transistor static random access memory cell has great read, write, and hold stability and uses very little power. A promising read stability yield is demonstrated by the 9T static random access memory cell when using Schmitt trigger inverters with single bit lines, according to this research. Additionally, Schmitt-trigger inverter writing assistance and other techniques have an impact on write ability yields. It is smaller and more efficient than the Schmitt-trigger 10-nm random access memory cell for 180-nm CMOS technology, and the MH 9-nm static random access memory cell.

Index Terms **-** *Bit interleaving, low energy, near-threshold, Schmitt-trigger, static random-access memory (SRAM).*

INTRODUCTION
Devices with a system on a chip (SoC), such as bioimplants, smartphones, wireless sensors, and energy harvesters, now place a high emphasis on low power consumption because of the limited energy they draw from batteries or minimizing the SRAM's power usage is one way to lessen the SoC's overall energy footprint [1]. Scaling back the supply voltage is the most efficient method of cutting back on power consumption (VDD). VDD is lower than Vth, and the delay increases exponentially in this region. As a result, even though the output power is very low, the energy consumption is significantly increased due to the significantly increased static energy consumption. Comparing sub-Vth operation to super-Vth, operating in the near-Vth region can save significant power and reduce latency significantly. This is because the VDD is slightly higher than the Vth in this region. Consequently, optimizing between power and delay can reduce power consumption in the near-Vth region [2].

Memory designers have come up with a variety of methods for reducing power consumption. With the rise in popularity of mobile phones and other portable electronics, there has been an increase in the need for the energy provided by SRAM cells. Because high-performance embedded processors require so much energy and die area, designing low-power SRAM is challenging. Because the memory's leakage current increases with capacity, standby power consumption rises. The most effective way to lower power consumption in memory devices is to reduce leakage current, among many others. It has been discovered a new Differential 10-transistor Schmitt SRAM bit cell with reduced leakage of 18% and read/write power of 50%.With subthreshold auto compensation, a 10-transistor SRAM cell's read and write SNM performance was considerably enhanced.

Voltage variations in the near-Vth region have a significant impact on the transistor's current output. When designing SRAM cells, small transistors are required for high density in a compact area. So, these SRAM cells are susceptible to this kind of fluctuation. Conventional 6T SRAM cells [3],[4],[5] cannot maximize both reading stability and writability at the same time due to a tradeoff between the two properties.

Write-back schemes are required for bit interleaving structures in SRAM cells because due to the high energy consumption and big size of SRAM cells. A novel layout for SRAM cells is introduced here that, in the near-Vth region, consumes less energy than previous designs while still preserving acceptable read/write stability when write-back is not necessary. Cross coupling between conventional and Schmitt trigger (ST) inverters enhances

legibility; second, the smaller area of the SRAM cell reduces energy consumption; and (3) reading stability by the application of ST inverters.

SRAM CELL DESIGNs

The 9T of the MHs [3], the 10T of Chang [4], the standard 8T [5], the 9T of WREs [6], the 10T of STs [7], and the 11T of STs [8] are among the SRAM cells that have been suggested for use close to the Vth in Figure 1. You can see these cells in Figure 1. Traditional 6T and 8T SRAM cells, along with Chang's 10T and MH 9T cells, utilize standard cross-coupled inverters. Rather, SRAM cells with built-in cross-coupling inverters, such as the ST 10T and ST 11T, are employed. Read disturbance at the storage node will cause the SRAM cells to be either read-disturbed or read-disturbed-free.

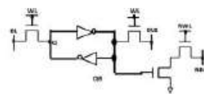


Fig 1: Conventional 8T SRAM cell

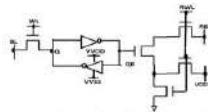


Fig 1: WRE 9T SRAM cell

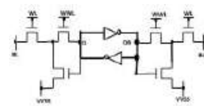


Fig 1: Chang's 10T SRAM cell

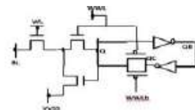


Fig 1: MH's 9T SRAM cell

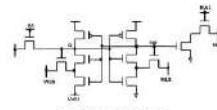


Fig 1: ST 11T SRAM cell

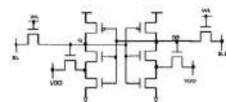


Fig 1: ST 10T SRAM cell

Fig. 1. The Previous SRAM Cell Schematics.

Traditional 6T SRAM cells are susceptible to read disturbances caused by BL and BLB, which can reverse the data stored within. As a default function, the read buffer is built within the 8T SRAM cell. When comparing read and hold stability, a conventional 8T SRAM cell is on par with a 4T cell. A stable readout is therefore provided by the 8T SRAM. WRE 9T SRAM uses power gating to reduce leakage current in the read buffer and increase writing capacity. Writing to standard 8T and WRE 9T SRAM cells causes BL or BLB read disruption, whereas writing to WRE 9T does not. Because write-back schemes are required when bit interleaving structures are used, the device's delay, energy consumption, and area are all significantly increased.

Integrating bits without write-back is crucial, and SRAM cells like ST 10T, MH 9T, ST 11T, and Chang's 10T are ideal for this use. Additional transistors connected in series to the pass gate make up the read buffers (PG) of a 10T SRAM cell. Along its journey down the column, a write word-line (WWL) signal governs the essential transistors. To help avoid issues caused by half-selected cells, a second transistor is turned off during write

operations. Thus, the half-selected cells in a row are no longer connected to BL. The read-disturbance cells are located in the ST 10T SRAM. The ST 10T SRAM cell is able to withstand read disturbances without causing data flips. There is a greater demand for space because of the increased transistor count and differential BL structure of the Chang and ST 10T and 10T SRAM cells.

PREVIOUS WORK

St 9t Sram Cell:

In Figures 2a and 2b, you can see the suggested single BL design for the ST 8T SRAM cell (see section below). A nMOS PG, three ST inverters (PUR, PDR1, and NF), and a regular inverter make up the proposed ST 8T SRAM cell. Word-lines can be divided into three categories: WL, WWLA, and WWLB. Row-based signals such as WL, while column-based signals such as WWLA and WWLB,exist. There are two connections to WL and one to WWLA for the gates of PUL2 and PG, respectively. WL and WWLA are connected. All of PDL1's gates and NF's sources are linked to WWLB.

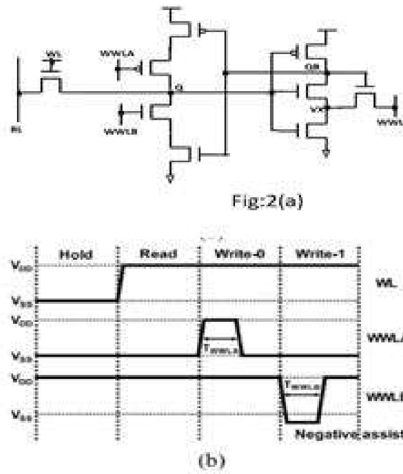
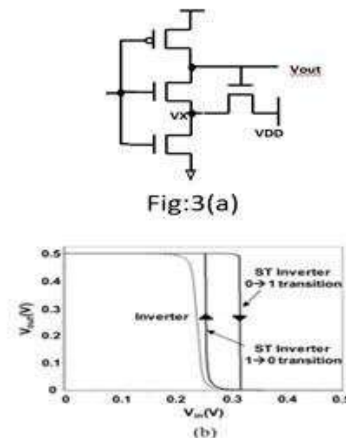


Fig.2. (a) Schematic, (b) The anticipated ST 9T SRAM cell operation timing diagram.

Fig. 3a and Fig. 3b show the ST inverter's schematic and DC characteristics, respectively (see figure 3a). One explanation for the variations is because ST inverters have a larger trip voltage compared to normal inverters. When the output power of PD1 is reduced by the feedback transistor NF, more VX is required. When compared to a regular inverter, a ST inverter can better withstand read disturbances.



A. READ OPERATION

By setting WWLB to 1 and WWLA to 0, the read operation activates PUL2 and PDL1, respectively. Storage node Q receives its electricity from the conventional inverter. It doesn't take long for the WL and the PG to be activated once they've been enabled. Whether or not the BL is discharged is determined by the data from Node Q. BL interference is a common cause of read failures. When the inverter's trip voltage bumps the storage node, it can cause data to be flipped due to read disturbances and higher inverter voltages. To address this issue, the ST 9T SRAM cell was recently developed. It employs a cross-coupled architecture that merges standard and ST inverters

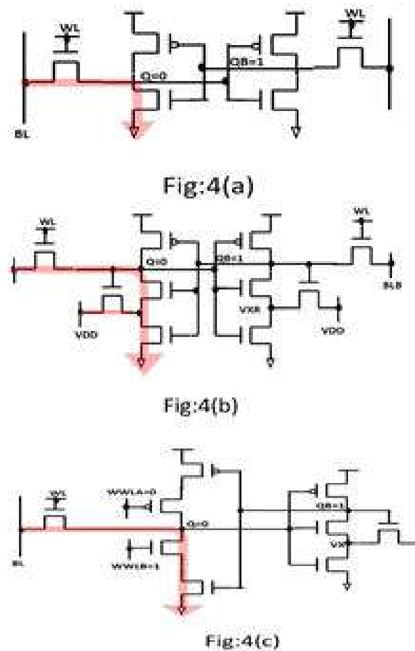


Fig. 4. "Read operation" in conventional 6T, ST 10T, and ST 9T SRAM cells respectively.

Bumping of storage nodes in read-disturbance cells is depicted in Figs. 4, 4, and 4a. The ST inverter improves the read reliability of ST 9T and ST 10T SRAM cells. By eliminating cross coupling between its SRAM inverters, the new suggested ST 9T SRAM cell makes for more reliable reads. That's because it serves a purpose. A read disturbance causes an increase in VXL and a decrease in PDL1 strength in a ST 10T SRAM cell. This causes more and more disruptions to the reading experience. The proposed ST 9T SRAM cell overcomes this problem by combining standard and ST inverses into a cross-coupled arrangement. In order to observe read disturbances, we set the value of the storage node in the single BL structure to zero.

B. WRITE OPERATION

Write operations vary according to the data being written. This is an example of a write-0 operation, as depicted in Fig. 5a. While a write is in progress, BL is always set to 1, even if the write driver has set it to 0. Disabling PUL2 by setting the column-based WWLA to "1" also cuts off power to the VDD. The power-gated Q node can be turned off by turning on the PG and then flipping the ST inverter switch. QB data must be flipped in order to reset column-based WWLA data. WWLA pulses need to take into account the column's half-selected cells (TWWLA). One PG is used to cut off access to VDD power when a zero is written to a ST 9T SRAM cell and PUL2 is deactivated. Using a ST 9T SRAM cell, which has been proposed, is feasible due to its sufficient write-zero capacity. In Figure 5 we see an instance of a "write-one" operation. (b). The write driver activates the WL in write-1 by assigning 0 to the column-based WWLA and 1 to the BL. In order to prevent access to the VSS power source, we must disable PDL1 and set the WWLB value depending on the column to "0". The ST inverter's tripping voltage can be reduced by removing the feedback mechanism. The power-gated Q node can be activated

by switching on the PG and then to the "1" setting on the ST inverter. The WWLB that is based on columns is reset to "1" whenever there is a reversal in node QB's data. The half-selected pulse from the selected cell in the second row is used to calculate this value. Removing the route from the VSS power source enables write-1 in the same way it enabled write-0. Reason being, NMOS PG's write-1 drivability makes writing one an unpredictable occurrence.

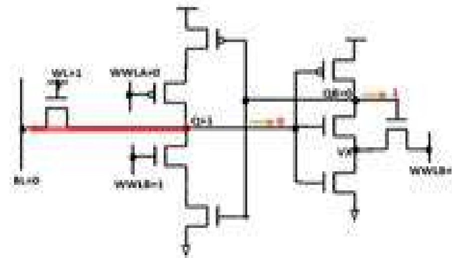


Fig:5(a)

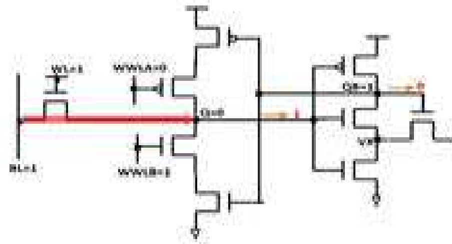


Fig:5(b)

Fig. 5. (a) Write-0, and (b) write-1 operations in the proposed ST 9T SRAM cell

PROPOSED WORK

Cell Design Concept:

Pictured in Figure 6 is a possible layout for an 8T ST SRAM cell. The memory cell's basic inverter pair has been optimized for low voltage operation in the proposed design. A pair of inverter transistors is formed by the transistors P11, P12, P13 and N11. The bit line's N11 and N21 access transistors are also employed. Schmitt trigger configuration is used to improve data reading stability when inverter stability is a major concern at low voltages (0 and 1). This design uses Schmitt trigger to alter the inverter's switching threshold based on the output transition's direction (PX or NX). The Schmitt trigger operation can be modified by employing a series transistor feedback technique.

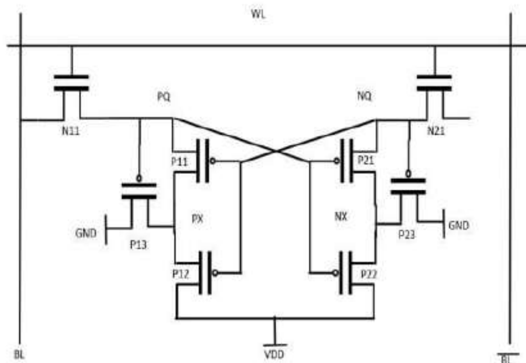


Fig:6

Fig. 6. Future 8-Terahertz ST SRAM Module.

READ AND WRITE OPERATION

As a result, when a memory cell's voltage divider is read, PQ (Q) voltage is altered. If the voltage across this inverter pair is higher than the voltage across the other inverter pair, data will be corrupted. In order to satisfy this criterion, the threshold voltage must be raised while storing "0" and "1" at PQ (Q) and NQ (NQ) (Q bar). These results are achieved using a method called pass transistor feedback (P13, P23). There is an improvement in both PX and NX thresholds that improves cell stability and prevents data failure during read cycles. In read mode, the circuit switches to zero potential BL and BL bar. When in read mode, the combined Q and Q bar lines' output potentials "1" and "0" are enabled by the positive edge trigger on the WL line. The BL and BL bar lines are read-only during writing operations. Labelled BL and BL bar for reading, the data output lines are Q and Q bar, while the control lines are BL. It allows error-free bit reading even at lower supply voltages. For example, some driver circuits are capable of connecting two bars together, which improves usability as well as the overall number of read/write lines. Table 1 summarizes the 8T ST SRAM cell design under consideration.

Table 1. An 8T ST SRAM Cell's Read/Write Operation Design.

Operation	BL	BL bar	WL	PQ (Q)	NQ (Q bar)	Operation	BL
Write ("1")	1	0	⎍	1	0	Write ("1")	1
Write ("0")	0	1	⎍	0	1	Write ("0")	0
Read	0	0	⎍	Stored output	Stored Output	Read	0

SIMULATION RESULTS 8T SRAM:

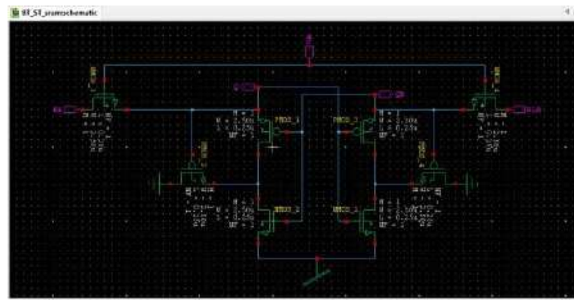


Fig. 7. Schematic design 8T SRAM

OUTPUT: Figure 8 depicts the read/write results of an 8T ST SRAM cell design. In order to simulate 0.18 m process technology, the Tanner EDA tool with support for SPICE is used.

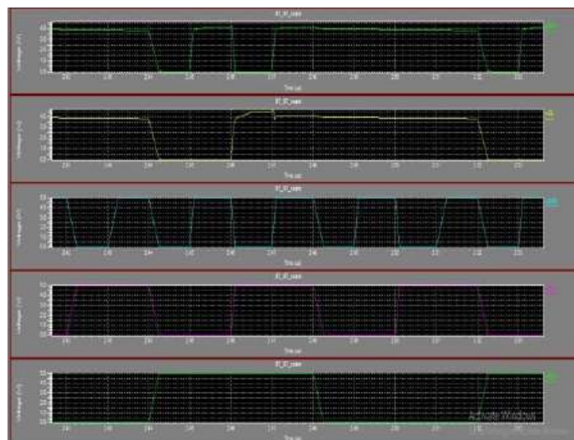


Fig.8 Simulated Read/Write Operation Results

9T SRAM:

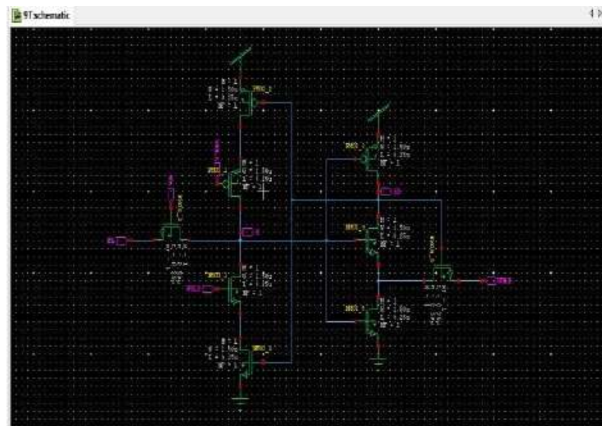


Fig. 9. Schematic design 9T SRAM

OUTPUT: Simulated data read/write operations are shown in Fig.10. In order to simulate 0.18 m process technology, the Tanner EDA tool with support for SPICE is used.

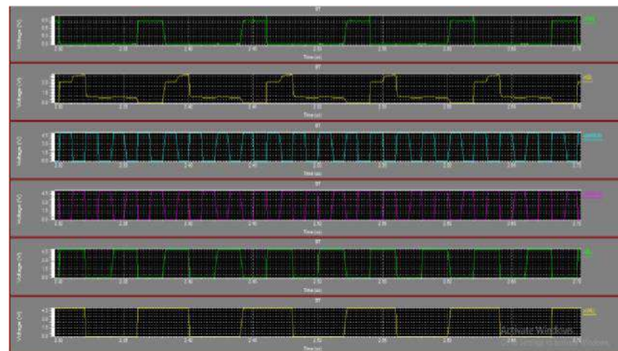


Fig.10 Simulated Read/Write Operation Results

Comparison Table:

	8T SRAM	9T SRAM
Area (T)	8	9
Delay (ns)	4.1	4.0
Power (uW)	13.7	23.9

CONCLUSION

The limited power supply of bio implants and mobile devices necessitates the use of low power devices. When operating in the near-Vth region of SRAM power consumption, it is essential. SRAM cells with Schmitt Trigger Logic (STL) can be designed with low power consumption by employing a novel methodology presented in this paper (8T ST SRAM). There is a comparison of this design's performance to existing methods. Only a tiny fraction of the power needed to run a typical memory cell is consumed by the new design. 8T ST-SRAM consumes less power because of a reduction in leakage current. Conventional 6T cells and 9T ST-SRAMs are compared using

0.18m process simulations. Low-power SRAM circuits can be implemented using this method. We believe our approach offers the optimal design for a microprocessor due to its consistent SRAM access and low power consumption.

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