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LEVERAGING COMPLEMENTARY CONTROL SIGNALS IN LOW-VOLTAGE ELECTRONIC CIRCUITS

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ABSTRACT

One of the central challenges in the realm of electronic circuits is addressing voltage loss, particularly in scenarios where the power supply voltage (Vdd) is low. In such situations, maintaining the quality of output signals becomes increasingly difficult, potentially leading to errors and inefficiencies in circuit operation. To tackle this issue head-on, this study explores the implementation of complementary control signals, which are signal pairs that are exact opposites of each other. When one is high, the other is low, and vice versa. These complementary signals prove to be instrumental in effectively managing voltage levels and mitigating the risk of voltage loss.

Keywords: CMOS, VLSI, p-type MOS and VDD

INTRODUCTION

The power consumption in CMOS (Complementary Metal-Oxide-Semiconductor) Very Large Scale Integration (VLSI) circuits primarily stems from the process of charging and discharging the capacitances of nodes within the circuit [1]. This phenomenon is commonly expressed as CV^2f power dissipation, where 'C' represents the capacitance, 'V' is the operating voltage, and 'f' stands for the switching frequency. Notably, this power dissipation is proportional to the square of the operating voltage, implying that even a small reduction in voltage can lead to significant power savings [2].

Reducing the operating voltage is a key strategy for achieving low power consumption in VLSI systems. As your source indicates, lowering the voltage from 5V to 3V results in a remarkable 64% reduction in power consumption [3]. This not only benefits power efficiency but also enhances signal integrity and reliability by mitigating issues like crosstalk and ground bounce.

For space systems, which demand both low power and high reliability, the transition to lower voltages is particularly appealing. However, there's a trade-off to consider – reducing the operating voltage can negatively impact circuit speed or throughput. This happens because lower voltages lead to slower transistor switching speeds [4-6].

POWER CONSUMPTION ANALYSIS

Power consumption analysis is a critical aspect of achieving low power and low voltage operation in VLSI systems. Understanding the sources of power consumption is fundamental to implementing effective power-saving strategies [7]. In this section discuss about dynamic power dissipation and static power dissipation.

Dynamic Power Dissipation

Dynamic power dissipation is a crucial concept in the operation of CMOS (Complementary Metal-Oxide-Semiconductor) circuits, which are commonly used in modern electronics. This dissipation occurs when MOS (Metal-Oxide-Semiconductor) transistors switch to charge and discharge the output load capacitance at the circuit's operating frequency.

Consider Figure 1, which illustrates a CMOS inverter with an output load capacitance. This inverter plays a fundamental role in digital circuits, where it transforms logical values (0 and 1) by switching between a pMOS (p-type MOS) transistor and an nMOS (n-type MOS) transistor. During the charge-up phase, when the input signal transitions and the inverter's output changes from 0 to VDD (the supply voltage), a specific amount of energy is

required to accomplish this transition[8]. This energy is drawn from the power supply and is momentarily stored in the output load capacitance. However, not all of this energy is efficiently used; some of it is converted into heat due to the resistance of the conducting pMOS transistor. This heat dissipation is what we refer to as dynamic power dissipation.

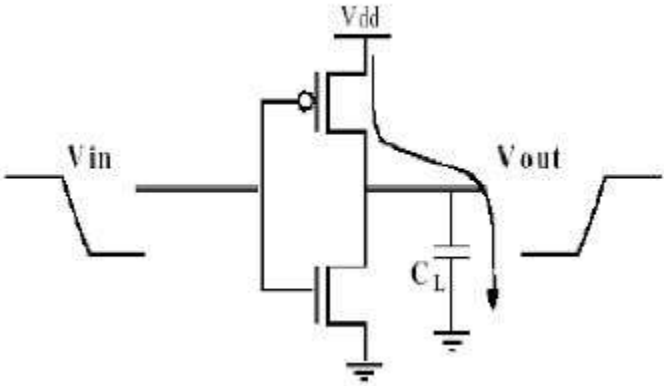

Figure 1: Charging **of output load capacitance CL**

The dynamic power dissipation at a specific output node can be quantified using

$$P_{dyn} = \frac{1}{2}.C_L.V_{DD}^2.F_{clk}.\propto$$

In a chip, there will be numerous output nodes, each with its unique load capacitance (C_i) and node transition activity factor (α_i), along with the associated charging voltage (V_i). Therefore, the total average dynamic power dissipation across all nodes can be expressed as:

$$P_{total} = \sum_i \left(\frac{1}{2}.C_L.V_i^2.F_{clk}.\propto_i\right)$$

Static Power Dissipation

Static power dissipation in a CMOS circuit due to leakage current, specifically focusing on the reverse leakage current in nMOS transistors.

In a CMOS circuit, when the circuit is in an idle state, meaning no dynamic switching activity is occurring, there is still a power dissipation known as static power. This static power is primarily a result of leakage current that flows through nominally off transistors [9]. Both nMOS (n-channel metal-oxide-semiconductor) and pMOS (p-channel metal-oxide-semiconductor) transistors used in CMOS logic gates have finite reverse leakage and sub-threshold currents.

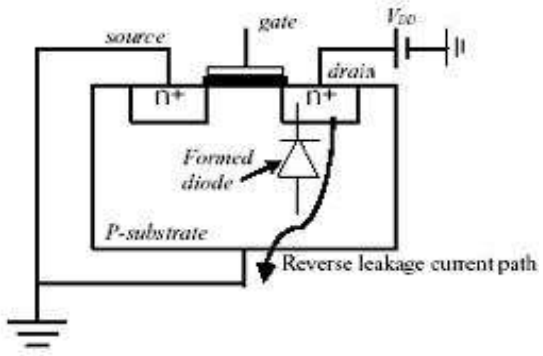

Figure 2: Diode-Induced Reverse Current Flow in CMOS Transistors

Let's focus on the reverse leakage current in nMOS transistors. The main component of leakage current in an nMOS transistor is due to the reverse-biased diode structure that exists within it. This diode structure comprises an n+ bar (n-type region) and the p-substrate (p-type region), forming the n-junction and p-junction of the diode, respectively [10].

The magnitude of this leakage current can be described by an equation. Let's denote the leakage current as $I_{reverse}$

The magnitude of the reverse leakage current (Ireverse) in an nMOS transistor can be described by the following equation:

$$I_{reversel} = A.D_n.\frac{n_i^2}{N_A}.\left(\frac{W}{L}\right).exp\left(\frac{V_{bi}}{V_T}\right)$$

Here, V_T represents the thermal voltage (approximately kT/q, where k is Boltzmann's constant, T is the absolute temperature in Kelvin, and q is the elementary charge).

This equation quantifies the leakage current in an nMOS transistor, which contributes to the static power dissipation in a CMOS circuit when the transistors are in the off state. The actual power dissipation due to leakage current in a silicon chip can be significant, especially when there are millions of transistors, making it comparable to dynamic power dissipation [11-13]. The specific values of leakage and sub-threshold currents depend on various processing parameters during the fabrication of the CMOS technology.

METHODOLOGY

One of the primary challenges in electronic circuits is dealing with voltage loss, especially when the power supply voltage (V_{dd}) is low. When the V_{dd} is low, it becomes more challenging to maintain the quality of the output signals. This degradation in output signals can lead to errors and inefficiencies in the circuit's operation.

To address this issue, proposed complementary control signals. Complementary signals are pairs of signals that are exact opposites of each other. When one is high, the other is low, and vice versa. These complementary signals help in managing the voltage levels more effectively and reduce the risk of voltage loss.

In the context of arithmetic circuits like adders, having complementary "propagate" control signals is particularly beneficial. These signals play a crucial role in controlling how data propagates through the circuit. By using complementary control signals, it's possible to minimize the degradation in output voltage swing. In simple terms, this means that the output signals stay closer to their ideal values even when the power supply voltage is low.

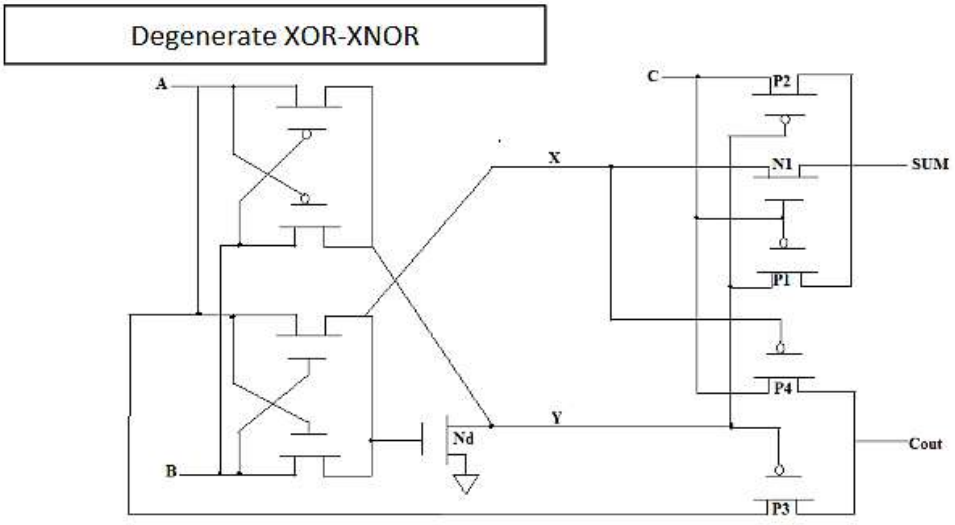

Figure 3: Proposed Architecture

Modified Transmission Gate Architecture

Transmission gates are electronic components commonly used in digital circuits. They are often referred to as pass gates because they allow signals to pass through or be blocked based on control signals. These control signals are typically complementary to each other, meaning that when one is active, the other is not.

A transmission gate consists of both an NMOS (n-channel metal-oxide-semiconductor) transistor and a PMOS (p-channel metal-oxide-semiconductor) transistor. These two transistors work together to act as a bidirectional switch between two nodes, labeled as A and B. The operation of the transmission gate is controlled by a signal called C, and its complement, denoted as Cbar (C or inverted C).

Here's how a Transmission Gate Works:

Control Signals: The NMOS transistor's gate is connected to the control signal C, while the PMOS transistor's gate is connected to the complement of C, which is Cbar.

High Control Signal (C): When the control signal C is set to a high voltage level (logic 1), it turns on both the NMOS and PMOS transistors. This means that there is a low-resistance path between nodes A and B. In other words, A and B are effectively connected, and signals can pass freely between them.

Low Control Signal (Cbar): Conversely, when the control signal C is low (logic 0), it turns off both the NMOS and PMOS transistors. In this state, the transistors provide a high-resistance path between nodes A and B. As a result, A and B are isolated from each other, and signals cannot easily flow between them.

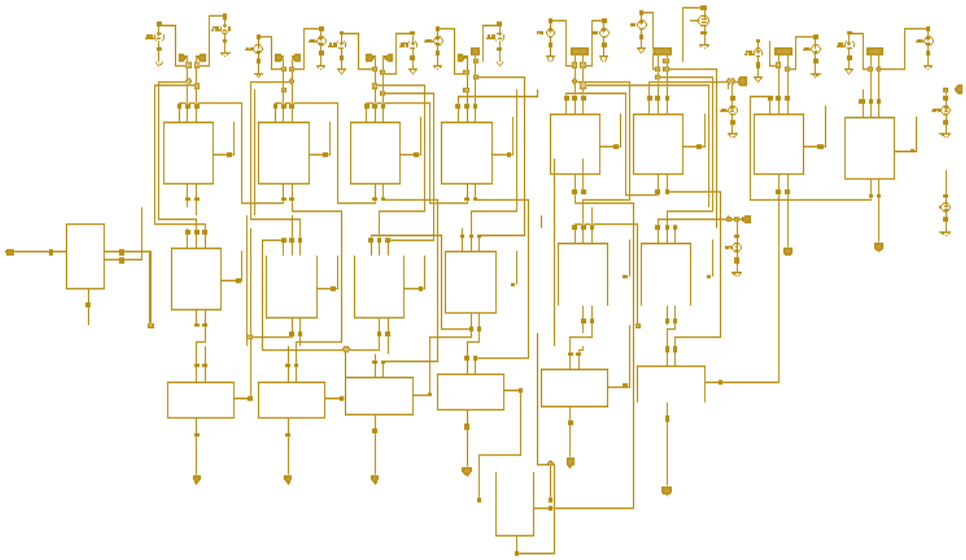

Figure 4: Efficient Full Adder Design Using Transmission Gates

RESULT

Based on our simulations and the systematic approach employed in constructing full adders using standard 10T and transmission gates, as well as binary to excess converter techniques, our study reveals significant advancements in electronic transistor adder designs. The newly improved transmission gate and 10T adder cells exhibit exceptional performance benefits, including significantly reduced power consumption within the order of small watts, a 46 percent increase in operational speed, and a 50 percent reduction in threshold loss, addressing critical issues in power efficiency, speed, and reliability. Additionally, the systematic approach results in improved transistor efficiency, making the adder design not only faster and more power-efficient but also more cost-effective to produce. These findings have the potential to greatly impact various electronic applications, making them more energy-efficient, faster, and more dependable.

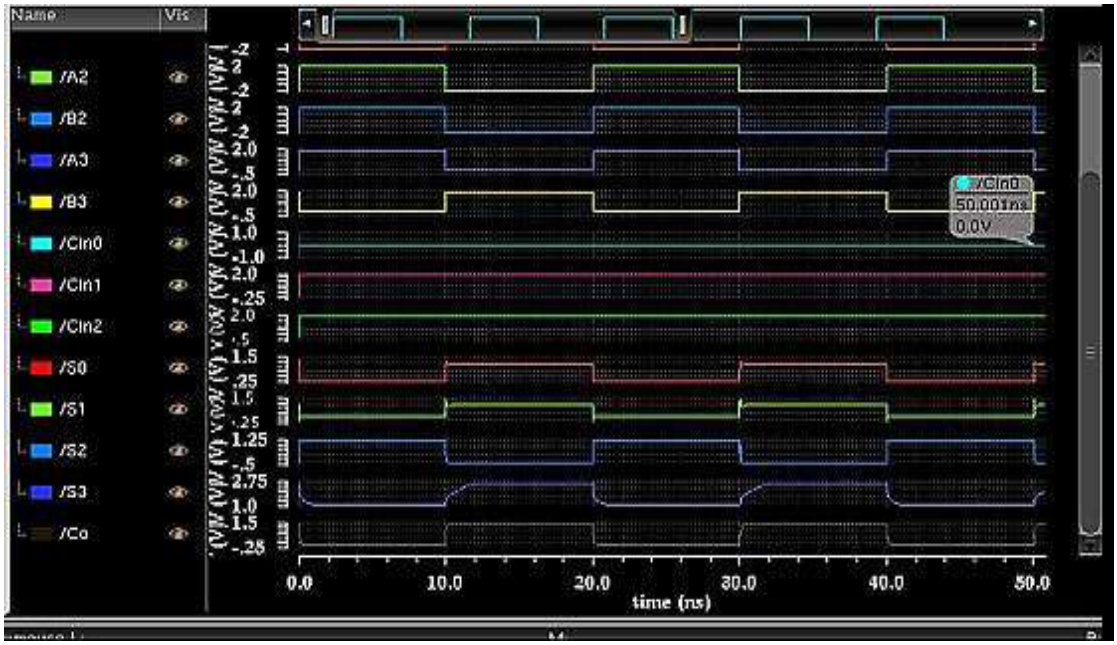

Figure 5: Simulation Result

CONCLUSION

The incorporation of complementary control signals represents a promising advancement in electronic circuit design, addressing the challenges posed by voltage loss and low Vdd scenarios. This approach not only ensures circuit reliability but also enhances signal quality and circuit flexibility, making it a valuable addition to the toolkit of electronics engineers working in power-constrained environments. As technology continues to evolve, the utilization of complementary control signals is poised to play a pivotal role in shaping the future of electronic circuitry.

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