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DESIGN OF METHODICAL AND ENHANCED PERFORMATIVE ADVANCED PHASE LOCKED LOOP WITH HIGH STABILITY EXTERNAL FREQUENCIES USING VLSI TECHNOLOGY WITH COMMUNICATION STANDARDS

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ABSTRACT

This paper presents a new design of advanced phase locked loop (pll) with multiple outputs with highly stable frequencies in the concept of low power consumption and high speed. The input frequency of 1 mega hertz, pll gotten external source is able to generate multiple frequencies provided for the circuits of communication standard in high-speed integrated circuits. The charge pump circuit will use the up and the dn signal to generate an output signal of cp for the control frequency of vco. The pll is designed with a 45nm cmos technology and verified under parasitic extraction. The results are elaborated when compared to the conventional design as lesser than 1mw power consumption and the out range of high frequency.

Keywords: phase locked loop, multiple frequencies, low power, radio frequency

INTRODUCTION

The recent and ongoing explosive growth of wireless communication systems require low-cost, low-voltage, and low-power transceivers. To utilize the advantages of scalability and performance (unity current gain cut-off frequency and noise figure), integration of RF and analog circuits with digital circuits in the advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology is promising, even under 0.5 V supply. Traditional phase-domain models of conventional charge-pump PLL can give an analogy for the ADPLL design. A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. PLLs are used to generate, stabilize, modulate, demodulate, filter or recover a signal from a "noisy" communications channel where data has been interrupted. Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock such as injection locking.

Monolithic phase locked loops have been used for clock- &-data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application. To deal with such complicated behaviours, a model-based analysis is often used because transistor-level circuit simulations for PLL take a too long time. This problem makes changes operate of the charge pump. The transistors switching not accurate effect to charge and discharge of capacitance. The current of the pull-up network will charge more than the pull-down network.

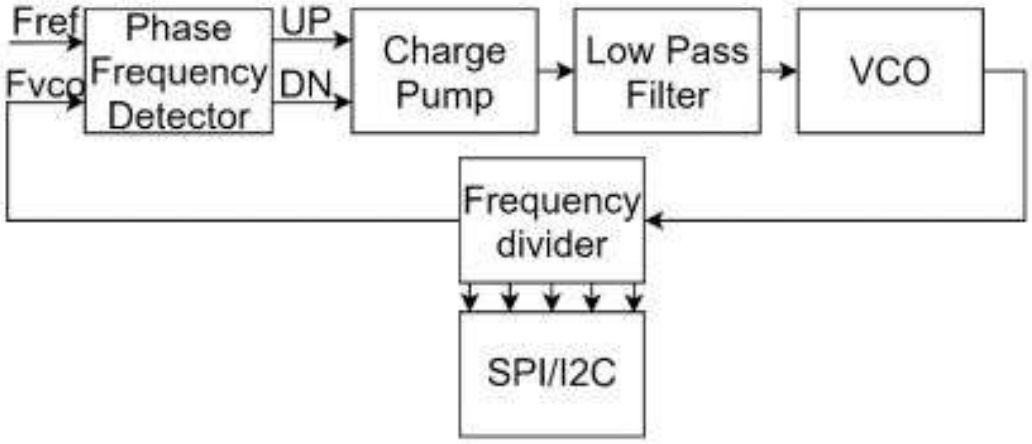

Fig. 1: Structure of Phase-Locked Loop

Phase Frequency Detector:

This circuit is responsible for comparing with two input signals and generating the waveform as the phase difference of the signals. There are two inputs, one from the output feedback of the VCO and one from the external reference input source. the Phase Frequency Detector use two D flipflop has been optimized for frequency 1MHz. If DFF has structure is D latch then delay of the signal due to RC parasitic on wire and switching of CMOS, detail of D flip flop shown in Fig.2 to reduce dead zone. This is a decisive issue for the PLL. This D flip flop can operate higher Frequencies and Lower Voltages.

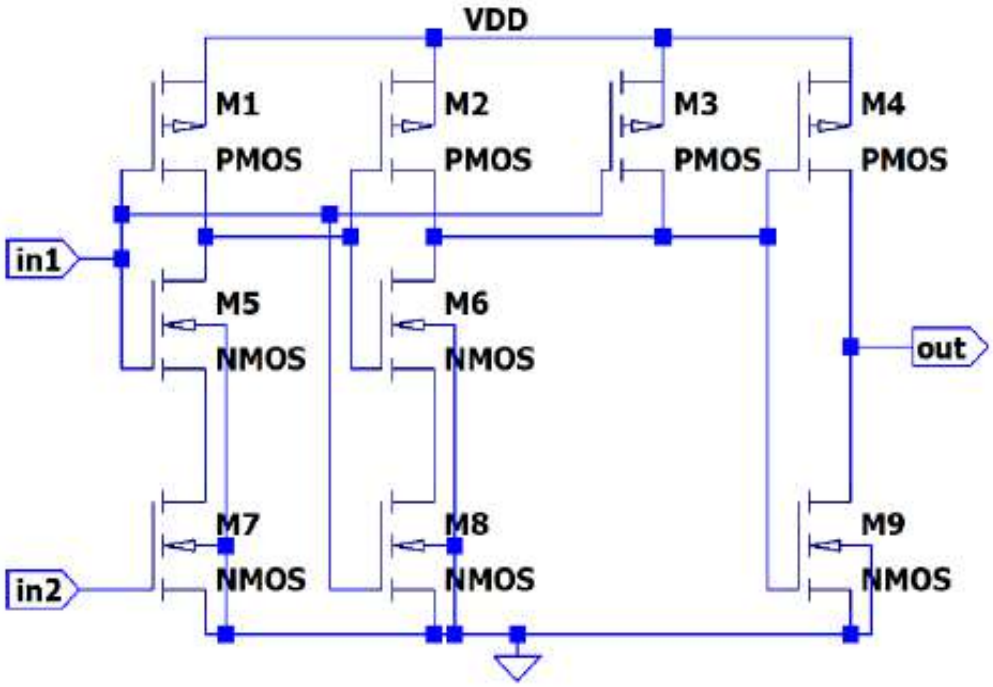

Fig. 2: Optimized D Flip flop Structure

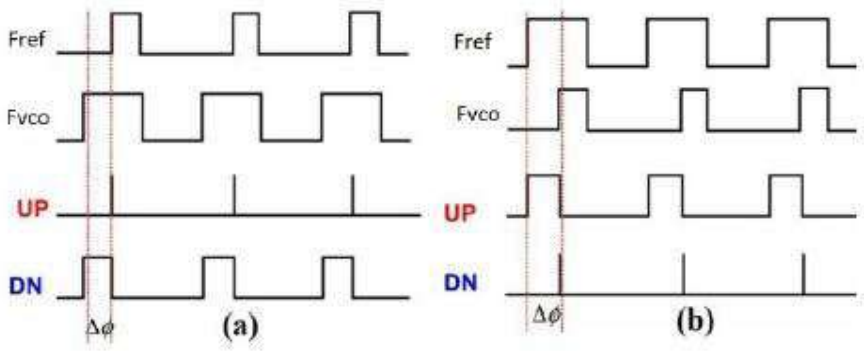

Fig. 3: Slow phase (a) and Fast phase (b)

The charge pump circuit will use the Up and Down signal to generate an output signal of CP for the control frequency of Voltage Controlled Oscillator. The output of Charge Pump goes to low pass filter for reducing noise. Low Pass Filter will filter the ripple of the high frequency and noises of charge (or discharge) to ensure stable and constant $V_{control}$.

Phase Locked Loop with Modified Voltage-controlled Oscillator:

The VCO block in the PLL is an important role circuit. It is an internal oscillator with a natural frequency that can be controlled by a control voltage at the time of the phase locking of the PFD circuit. The example at voltage A, the VCO will produce the output oscillation frequency A', at the input voltage level B, the VCO will produce the output oscillation frequency B'.

The phase-lock-loop (PLL) is commonly used in microprocessors to generate a clock at high frequency (Fout=5GHz for example) from an external clock at low frequency (Fref=500MHz for example). Clock signals in the range of 1GHz are very uneasy to import from outside the integrated circuit because of low pass effect of the printed circuit board tracks and package leads. The PLL is also used as a clock recovery circuit to generate a clock signal from a series of bits transmitted in serial without synchronization clock. The PLL may also be found in frequency demodulation circuits, to transform a frequency varying waveform into a voltage. The PLL uses a high frequency oscillator with varying speed, a counter, a phase detector and a filter as shown in above figure.

Design of VCO Using 45 nm Technology:

The layout of VCO which is develop by us is a modified design of high performance VCO. This is a optimum design for use in industries at 45 nm VLSI technology. In the estimated design more emphases is given on power consumption, layout design and many more. Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The high performance VCO provides very good linearity as compared to previous one.

In Microwind, the threshold and mobility parameters are varying with a normal distribution <Gloss>, with a typical variation of 10%. The delay dependence on $V_{control}$ is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point Vc. The rise edge is almost unchanged. Simulation of VCO layout is taken for frequency Vs time graph with timescale of 5nsec. The frequency obtained for VCO is 6.21 GHz. By increasing the number of inverters and altering the size of the MOS current source, we may modify the oscillating frequency very easily.

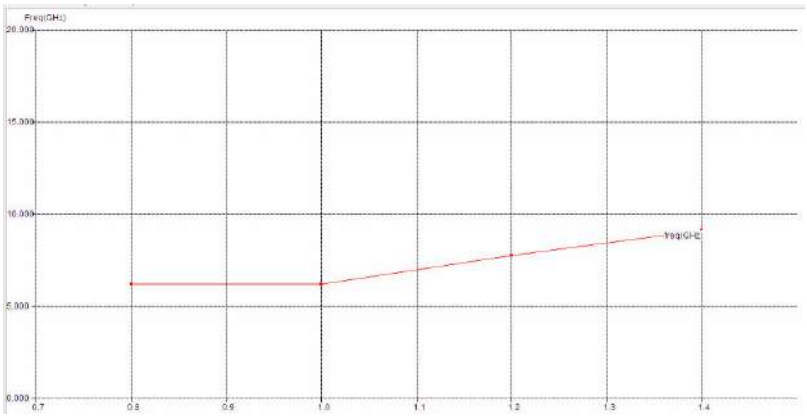

Fig. 4: Voltage variation of V_{DD} verses frequency of node V_{high}

Result Analysis of Advanced PLL with Improved Stability Coditions:

For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The modelling of CMOS device behaviours is analysed with the equations including threshold voltage, short channel effect narrow channel effect, electron temperature effect, hot carrier effect and capacitance model. Finally, the BSIM SPICE models BSIM4 are summarized for deep-submicron CMOS transistor. For low power, low leakage transistors BSIM4 are used and compromised on little bit frequency. Also, there is shutdown input in proposed circuit which brings the PLL to hold. BSIM4 model of the transistor NMOS and PMOS is having the specifications as follows:

Here for the design, microwind 3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed Advanced Phase Locked Loop is designed, which in turn offers high speed performance at low power. This layout design is implemented using 29 NMOS along with 28 PMOS BSIM4 transistor-based rules of software. The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of VDD emerges as a very effective means of limiting the power consumption. For the proposed PLL, power supply VDD of 1 volt is used. Figure.5 shows the results of optimum, highly efficient chip design of low power PLL with multiple (Four) output using 45nm VLSI technology.

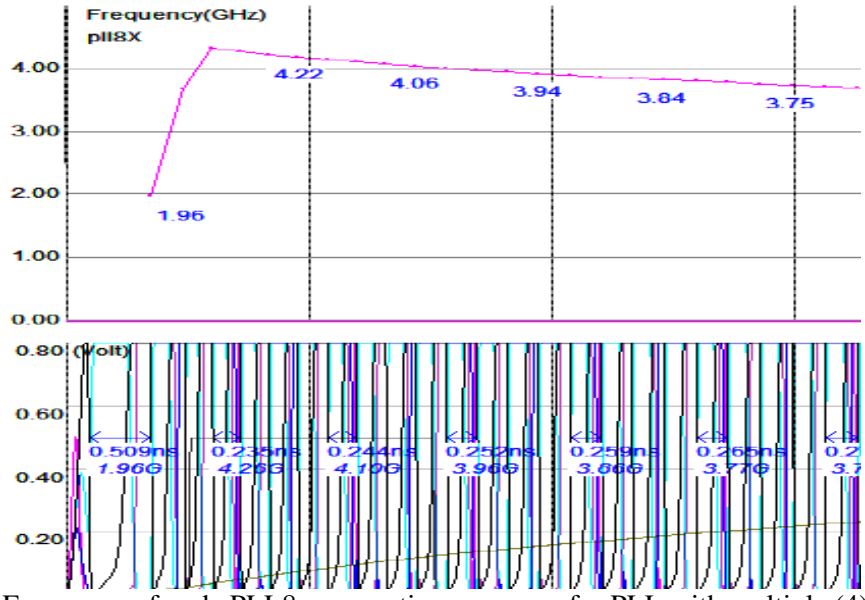

Fig. 5: Frequency of node PLL8x verses time response for PLL with multiple (4) output

Since the PLL, provide multiple clock generation, it is a research problem to design PLL using 45nm process technology parameters which will offers high speed performance at low power. Optimum layout for high frequency PLL is designed using high performance VCO, which is almost stable when Vc reaches to 0.501 volt. From the parametric analysis of design tool shown in fig 6, it is observed that the power dissipation measured by VDD at 1Volt is found 0.113miliwatt, which shows that power consumption is very low.

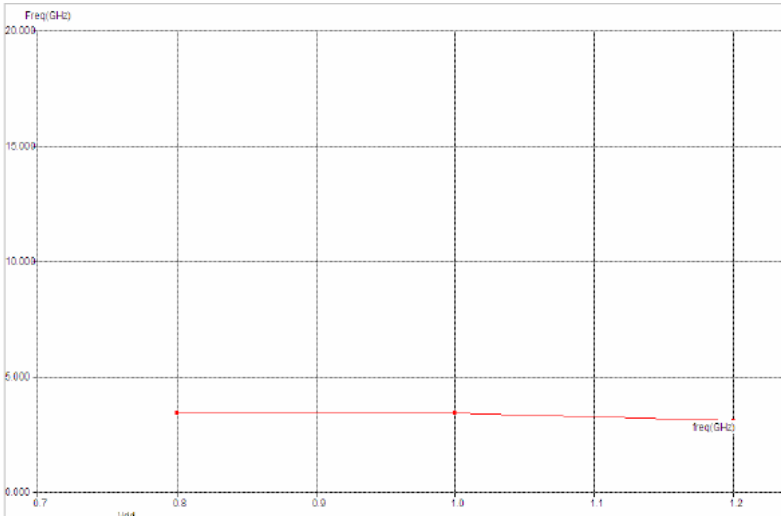

Fig. 6: Voltage variation of vdd verses frequency of node Vhigh for PLL with multiple (4) output

As a result of technology scaling, there are increased process variations of circuit parameters such as the transistor channel length and transistor threshold voltage. The increased process variations can have a significant effect on circuit performance and power variations also have an impact on how exactly a parallel system should be designed. This layout design is implemented using 29 NMOS along with 28 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the lambda based rules of microwind 3.1 software.

Temperature	Frequency
25°	128 MHz
31.25°	127 MHz
37.5°	125 MHz
43.75°	124 MHz
50°	122 MHz

Table 1: Simulation of VCO with generated temperatures

CONCLUSION

The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of VDD emerges as a very effective means of limiting the power consumption. For the proposed PLL, power supply VDD of 1 volt is used. Figure shows the optimum, high efficient chip design of low power PLL with multiple (Four) output using 45nm VLSI technology. the optimum, high efficient chip design of low power PLL with multiple (Four) output using 45nm VLSI technology. The PLL has used techniques such as mismatch avoidance in the CP, proposed a new architecture for the DFF, reduced noise for the VCO with bias network, and current mirror. Nowadays, the Micro ICs are developing, so application variety of the PLL in the wireless sensor network, communication with the server based standards.

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