ISSN: 2633-4828 Vol. 5 No.4, December, 2023

International Journal of Applied Engineering & Technology

# SIMULATION ASPECTS OF LOW POWER ENERGY EFFICIENT PHASE FREQUENCY DETECTOR EMPLOYED IN PLL – 45NM CMOS PROCESS

**Ravi Kumar M[1] and Dr. U. Eranna[2]**

[1]Research Scholar, Department of Electronics and Communication Engineering, BITM Research Center, Ballari, Karnataka, India

[2]Professor & Dean (SW /FW), Department of Electronics and Communication Engineering, BITM Research Center, Ballari, Karnataka, India

[1] mravikumar.vlsi@gmail.com and [2] jaya88veer@gmail.com

## ABSTRACT

*The primary goal of the project is to construct a complete phase-locked loop (PLL). In electronic and digital communication, PLL plays a crucial function. Both analog and digital circuits are capable of supporting PLL implementation. The phase locked loop's primary useful application is mainly centred on clock production and recovery in microprocessors, Communication systems, digital networking, and frequency synthesisers. Phase locked loops are most frequently used in high performance digital systems to create precisely timed on chip clocks. Phase Locked Loop is mainly utilized in contemporary wireless communication systems for synchronization, clock synthesis, skew minimization, and jitter minimization. A PLL circuit with quicker locking capability is required since circuit operation speed has increased. In today's communication systems use frequencies in the GHz range. Thus, PLL must function in the GHz band with shorter lock times. Due to the PLL's architecture, which combines digital and analog signal processing units, it is a mixed signal circuit. The effort focuses on redesigning a PLL system utilizing CADENCE Virtuoso Analog Design Environment using a 45 nm manufacturing technology. The better performance of a current-starved ring oscillator in terms of their small chip area, low power need, and broad tunable frequency range has been taken into consideration for this application. The layout structure of PLL is created using the CADENCE Virtuoso XL Layout editor.*

*Keywords: PLL, voltage-controlled oscillator (VCO), a phase frequency detector (PFD) cadence virtuoso, skew and jitter.*

## INTRODUCTION

The PLL concept was first presented in the 1930s, and since then the range of PLL applications has expanded and drawn numerous designers. The desire to work in this subject has grown as technology has advanced and new designs, issues, and non-ideals have emerged. The world of electronics and communication has several uses for PLL.

PLL is typically used to generate clocks for microprocessors, as a frequency synthesizer in mobile devices, etc. Phase locked loops are used in a variety of circuit types. There are many different uses for them. Clock synchronization, demodulation, jitter and noise minimization and also de- skewing are just few of the any fields in which it can be used in.

A PLL must compare its operating frequency to the clock frequency in order to operate, and it must then adjust its output to match the input. The fundamental structure of a PLL must be discussed and looked at in order to properly comprehend how this PLL process functions. A PLL is .characterized as a feedback mechanism that evaluates the relationship between the input and output phases. A "phase comparator" or "phase detector" does the comparability (PD).

## COMPONENTS

Regardless of the PLL's use, there are primarily three components that are present. As demonstrated in Figure 1, these components consist of a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), and lastly low-pass filter.

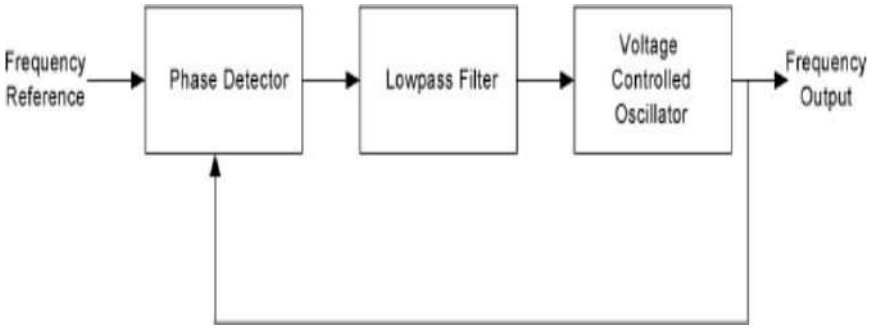


**Fig 1:** General formation of Phase Locked Loop

### A. Phase Detector

A phase detector, which is the first component and is essential to the operation of the system, can be divided into two types: a 6 phase only detector and a frequency and phase detector. Only the phase difference between two distinct signals with the same frequency can be detected by a phase detector. The input signal and the return signal, which are both distinct signals, are contrasted by a frequency and phase detector, which establishes the differences in phase between the signals. The subsequent phase receives an "error" voltage that is translated from the phase and frequency discrepancy.

### B. Low pass Filter

A filter with a low pass and narrow band makes up the following component. It eliminates any high-frequency components from the phase frequency detector's signal output and delivers a fixed voltage signal to the VCO.

### C. Voltage Controlled Oscillator

The VCO generates the second signal that will be measured with the input signal. The voltage signal which emerges from the phase detector after filter processing , controls it. Depending on the requirements of the circuit, the VCO design may differ. The requirements can differ substantially depending on whether you're constructing a low noise, low power, or simple oscillator.

## DESIGN AND RESULT OF PLL

### A. Phase Frequency Detector

In PLL circuits, one of the key components is the Phase frequency Detector (PFD).

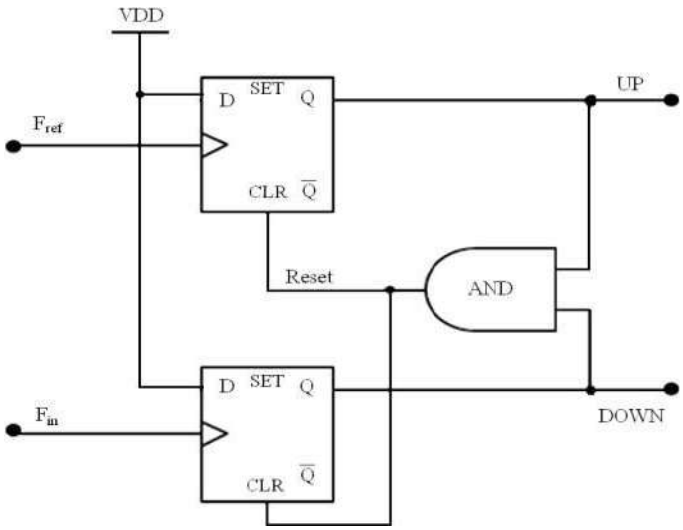


**Fig 2:** Traditional PFD circuit diagram

The feedback clock's and the reference clock's phase and frequency discrepancies are contrasted. In accordance with variation in phase and frequency, it emits two output signals, UP and DOWN. In Figure 2, a typical PFD circuit is displayed. Depending on whether or not the given difference in phase between the two signals, they will emit up or down synchronised signals. The UP-signal increases while the DOWN signal remains low when the reference clock's rising edge arrives after the clock's rising edge driving the feedback input. In contrast, the DOWN signal will rise high and the UP signal will fall low if the feedback input clock rising edge occurs before the reference clock rising edge. In contrast to quick PFDs, slower PFDs are frequently selected for phase and frequency acquisition. Fig 3, depicts the typical test bench for the phase detector.

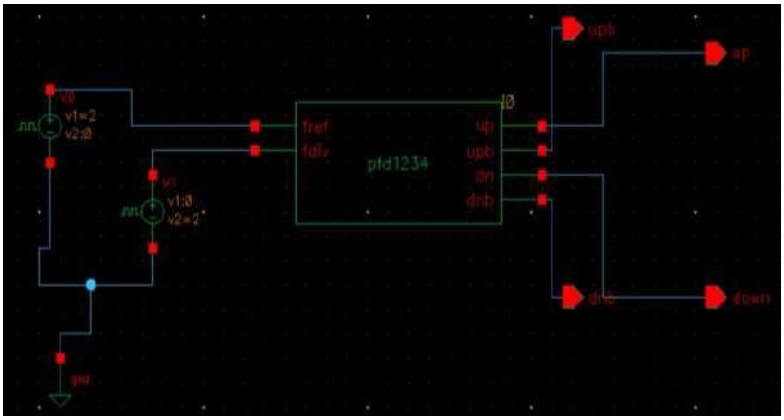


**Fig 3:** Test Bench of PFD

### B. Charge pump

An essential element of the entire PLL system is the charge pump component.It transforms the information about the frequency or phase difference into the voltage that is utilised to adjust the Voltage controlled oscillator. The PFD's two outputs are combined into one output, which is then delivered into the filter's input, using the charge pump circuit.The IPDI constant current produced by the charge pump circuit should be unaffected by changes in the supply voltage. Although the current's polarity fluctuates depending on the strength of the "UP" and "DOWN" signals, its amplitude always remains constant. Figure 4 below shows the charge pump test bench.

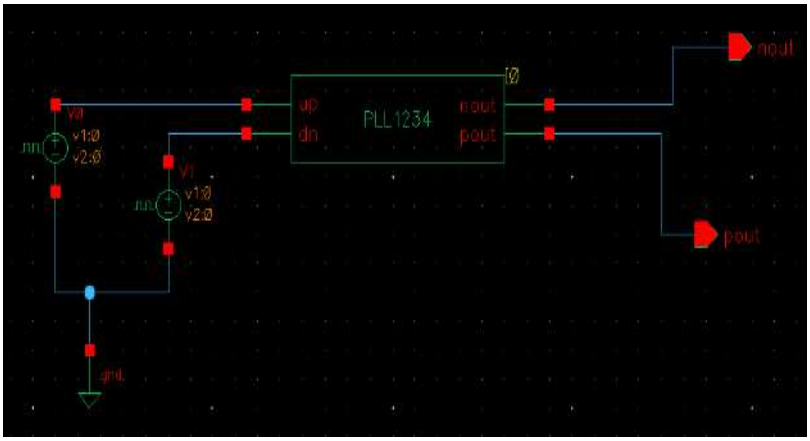


**Fig 4:** Test bench of charge pump

### C. Low-pass filter

The low pass filters are frequently installed behind the charge pump to minimize distortion. The loop filter, which further minimizes high frequency noise introduced by the phase frequency detector, converts the phase frequency detector's output signal into control voltage. Figure 5 depicts a common low-pass filter as the loop filter for this type of PFD.

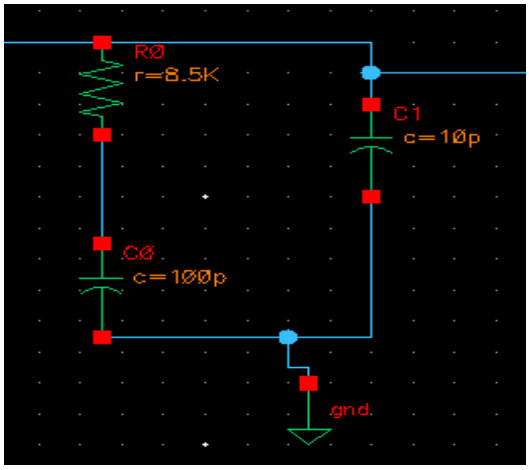


**Fig 5:** Test bench of low pass filter

### D. Voltage Controlled Oscillator

The voltage-controlled oscillator happens to be among the most essential fundamental building blocks in both analogue and digital circuits (VCO). In a ring oscillator with many delay stages, the output of the last delay stage is fed back into the first delay stage. The ring must have a phase shift of 2 and a unity voltage gain at the oscillation frequency in order to cause oscillation. The test bench for the VCO is seen in Figure 6 below.

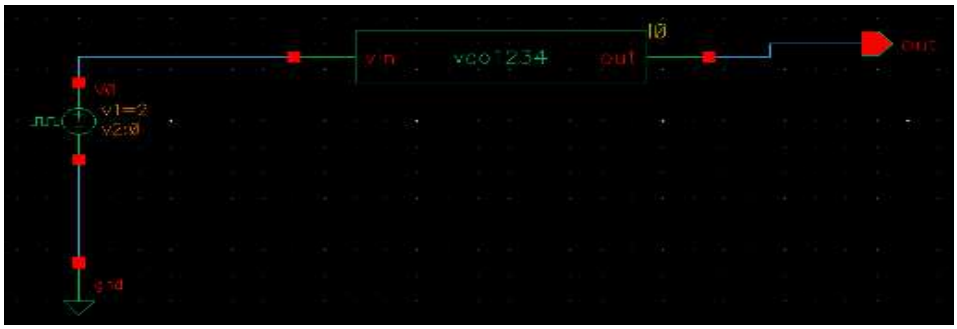


**Fig 6:** Test bench of VCO

### E. Frequency divider

The CS VCO's output has been sent back to the PFD'S input of the using the frequency divider circuit. A closed loop is produced by the frequency divider in the PLL circuit. After the phase frequency detector, the charge pump is a structural component that lowers the frequency of the CS VCO output signal. The frequency divider test bench is seen in Figure 7 below.

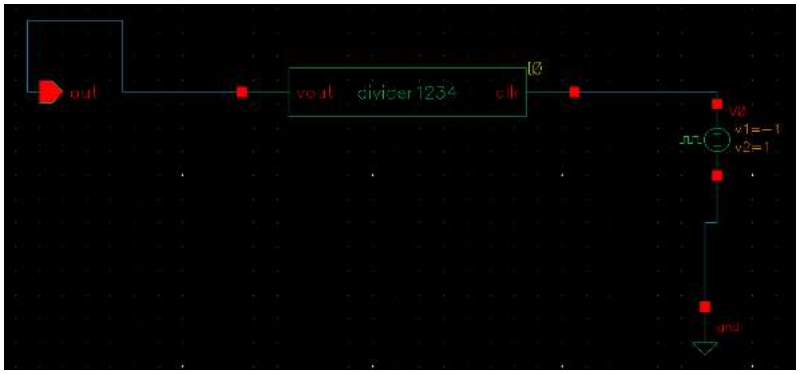


**Fig 7:** Test bench of frequency divider

### F. Results of PLL

The PLL schematic, its test bench, and multiple PLL waveforms in various stages are shown in the pictures below.

### G. Schematic of PLL

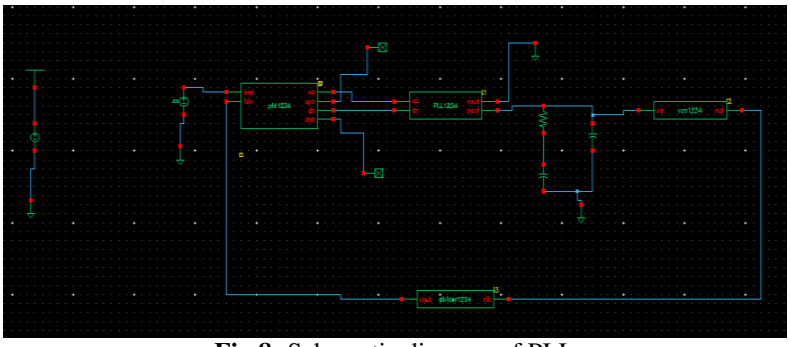

**Fig 8:** Schematic diagram of PLL

Figure 8 depicts the four main PLL building blocks: charge pump, frequency divider, phase frequency detector and VCO. Moreover, this block has a low pass filter. The whole PLL waveform is seen in the image below.

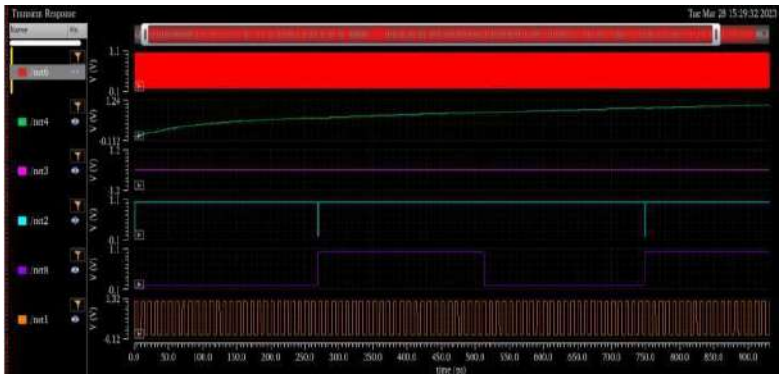

**Fig 9:** complete PLL circuit waveform

Table 1 lists the results of the PLL simulation performance with the parameters.

**Table 1:** Simulation results of PLL

| Parameter | Result of Simulation |
|---|---|
| Technology | 45nm |
| Power Supply | 1.8 V |
| Frequency | 100MHz |
| Phase Noise | -6.4 dB |
| Slew rate | 12.0 V/ns |
| Area | 21.54% |
| Power consumption | 34.3uW |

## CONCLUSION

In this work, a PLL with a superior design for CMOS 45nm technology is described. In this project, we developed a number of PLL building components, including the frequency divider, charge pump, voltage-controlled oscillator and phase frequency detector. The PLL is determined to have a power of 34.3uW which improves efficiency. The developed PLL is therefore an energy-efficient PLL, allowing us to utilize it in a variety of applications.

## REFERENCES

[1] S. Aditya and S. Moorthi, "A low jitter wide tuning range phase locked loop with low power consumption in 180nm CMOS technology," *2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia)*, Visakhapatnam, India, 2013, pp. 228-232, doi: 10.1109/PrimeAsia.2013.6731211.

[2] Y. Han, Q. Zhang, C. -K. Li and X. -D. Li, "Analysis of the Influence of the Loop Filter in the Phase Locked Loop on the Output Phase Noise," 2018 15th International Computer Conference on Wavelet Active Media Technology and Information Processing (ICCWAMTIP), Chengdu, China, 2018,pp.185-189,doi:10.1109/ICCWAMTIP.2018. 8632591.

[3] A. Mann, A. Karalkar, L. He and M. Jones, "The design of a low-power low-noise phase lock loop," *2010 11th International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, USA, 2010, pp. 528-531, doi:10. 1109/ISQED.2010.5450522.

[4] Mann, A. Karalkar, L. He and M. Jones, "The design of a low-power low-noise phase lock loop," 2010 11th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, USA, 2010, pp. 528-531, doi: 10. 1109/ISQED.2010.5450522.

[5] D. Bhati and B. Singh, "Design and Analysis of a Low Power Digital Phase Locked Loop," 2016 8th International Conference on Computational Intelligence and Communication Networks (CICN), Tehri, India, 2016, pp. 275-279, doi: 10.1109/CICN.2016.60.

[6] S. Hokrani, T. C. Thanuja and K. V. Kumaraswamy, "Design and implementation of Phase Locked Loop on 180nm Technology node," 2018 4th International Conference for Convergence in Technology (I2CT), Mangalore, India, 2018, pp. 1-6, doi: 10.1109/I2CT42659.2018.9057996.

[7] G. Bhargav, G. Prasad, S. Datta Canchi and B. Chanikya, "Design and analysis of phase locked loop in 90nm CMOS," 2016 Thirteenth International Conference on Wireless and Optical Communications Networks (WOCN), Hyderabad, India, 2016, pp. 1-7, doi: 10.1109/WOCN.2016.7759029.

[8] P. T. Patil and V. Ingale, "Design of a Low Power PLL in 90nm CMOS Technology," 2019 IEEE 5th International Conference for Convergence in Technology (I2CT), Bombay, India, 2019, pp. 1-3, doi: 10.1109/I2CT45611. 2019.9033824.

[9] Ravikumar Mugadhanam, Eranna Uppara Low Power FMCW Transceiver Design With 140- ghz in CMOS 45nm Technology, *2020 IEEE International Conference for Innovation in Technology (INOCON) Bengaluru, India. Nov 6-8, 2020*

[10] Ravikumar Mugadhanam, Eranna Uppara Design and Analysis of Improved 3-Stage LNA Architecture for CMOS RF Front End Receiver Systems, *International Journal of Intelligent Engineering and Systems, Vol.15, No.3, 2022* DOI: 10.22266/ijies2022.0630.02

[11] Ravi Kumar.M, Dr.U.Eranna ―A comprehensive study on Design Implementation of CMOS Low Noise Amplifier published in GRJ, Volume-9,Issue-1,pageno:1028-1035,2023. DOI:10.37897.GRJ.2022.V8I12.22.5071.

[12] Ravi Kumar.M, Dr.U.Eranna, ―An efficient Design Implementation of OFDM Based Transmission system‖, IJSTR-Elsevier Scopus approved journal, INTERNATIONAL JOURNAL OF SCIENTIFIC & TECHNOLOGY RESEARCH VOLUME 8, ISSUE 11, NOVEMBER 2019 ISSN 2277-8616 https://www.scopus.com/sourceid/ 21100894501