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DEVELOPMENT OF REAL TIME HIGH SPEED DATA ACQUISITION SYSTEMS FOR UNDERWATER FLOW NOISE MEASUREMENT

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ABSTRACT

The implementation of high-speed real time data acquisition system, which can be used for measurement of underwater flow noise. In the system, Virtex-5 FPGA is used as main controller, HDL coding is implemented and tested for acquisition, processing and storing of acoustic sensor elements data at higher speeds. It is an on-board DAQ system which can be mounted in the under water systems for flow noise measurement. The system acquires 32 channels of sensors data, processes it and saved into the on-board memory for post-trial data analysis. The system is interfaced with USB for data monitoring and offline data retrieval. The higher sampling rate of 180MSPS is achieved for 32 channels. In order to retrieve and analyze the data, an analysis software is coded in C++ in visual studio. The system is well suited for field trials of underwater vehicles to characterize the channel.

Index Terms – Data acquisition and FPGA; High Speed system.

INTRODUCTION

Data acquisition is an essential part in all communication and control application. Flow noise is one of the main interference noise that limits the performance of sonar for under water applications. The noise reduces the signal to noise ratio and shortens the sonar detection range or transmission range of sonar signals. The flow noise is measured to estimate the noise floor of the specific under water stream. It is required to have very high speed Data Acquisition Systems (DAQ) for the measurement of flow noise to estimate the performance in the design of any acoustic communication systems or to characterize the acoustic communication channel. Data acquisition hardware is implemented with programmable devices such as field-programmable gate arrays. In order to obtain analog data, a low-pass filter is used which removes the high-frequency noise, after which the filtered signal is given to an Analog to Digital converter [1]. All ADC's are simultaneously initiated through an FPGA interface that these ADCs are interfaced to. Once converted, the ADC data is read from the nonvolatile memory and is saved to the FPGA.

There are a number of methods of data acquisition in which converting physical phenomena from the real world into electrical signals. The measurements and conversion of these signals into a digital format are done by Data Acquisition system using Analog to Digital Converter. The data acquisition system is categorized into two distinct types depending on the onboard storage capacity. DAQs with internal storage are especially well suited for field applications [2]. A number of automatic test and measuring instruments make use of the data acquisition system. Peripheral input devices, such as transducers, sensors, and other subsystems, can be integrated with these systems. This measured data must be saved for further analysis. Compared to microprocessor-based data acquisition systems, FPGAs provide a very effective solution because of parallel execution, reconfigurable, and no separate glue logic. An FPGA-based system can allow higher data transfer speeds [3].

DESIGN ASPECTS

The proposed system design is divided into three major components PC test station, Front-end electronics with sensors and multi-channel acquisition with on-board memory. This block diagram illustrates the design of the FPGA-based data acquisition system. The front end electronics are interfaced with the piezo-electric sensors for acquisition of acoustic signals. The differential signals from the sensors are given to low-noise pre-amplifier to increase the signal levels to acquire and store the data. To eliminate low-frequency noise, low-pass filters are designed [4].

Signal conditioning circuit that is a sixth order low pass filter has a differential analogue with 35 KHz cut-off frequency. The ADC is interfaced with FPGA controller to acquire and process the signals. Multiple ADCs are interfaced to FPGA and simultaneously all ADCs are initiated and data can be retrieved with fast rates [5]. Therefore, FPGA is better option for high-speed data acquisition and processing. Virtes-5 FPGA is used as a controller and the data from ADC is stored in NAND Flash. In order to boot the FPGA from serial Flash, for every power on, the FPGA is interfaced with boot flash. The USB is used to interface with a PC for communicating and online data monitoring.

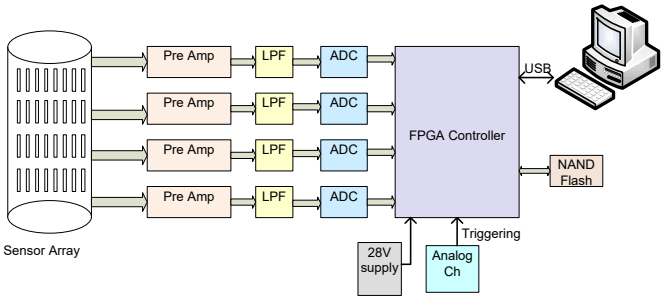

Figure.1. Block Diagram of the Daq.

IMPLEMENTATION

An FPGA generates the control sequence necessary for all of the connected devices. NAND Flash is utilized to store data acquired and processed by an FPGA controller after which it is saved in the NAND [6]. The necessary processing algorithms is implemented in host PC with MALAB on the received data. The data is also analyzed for sonar image detection from the sensors array data [7]. The main architecture of the peripherals with controller is shown in the figure.2. The controller initiates the ADC acquisition and storing of the time stamp values derived from FPGA clock with acquired data into the block RAM. Once BRAM memory is filled, data is transferred from BRAM to the USB FIFO. The AD7655 may be run from a single 5 V supply and is available in the form of a 5 V or 3 V digital logic interface [8]. The ADC has a maximum throughput of 1MSPS while in standard mode. Serial data is multiplexed on the parallel data bus.

When the Serial or Parallel signal is held high, the AD7655 is setup in the slave serial interface. The AD7655 outputs 32-bit data, with the MSB output on the SDOUT pin. The 32 clock pulses for the SCLK signal are used to sync this data. The system is operated with DC supply of 28V and switched on by main power distribution controller. The DC-DC Converter derives the necessary supply voltage of +5V. Other necessary voltages for peripherals are derived from switching regulators.

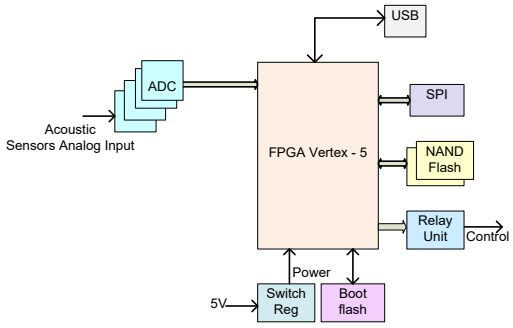

Figure.2. FPGA Controller Interface

DIFFERENTIAL AMPLIFIER DESIGN

Flownoise generated in under water communication systems is very low and weak. The weak signal cannot be given directly to ADC. The signal must be amplified to fit to the ADC input range and filtered to remove low frequency noise [8]. It is built up of a fixed-gain, low noise instrument amplifier, a sixth-order low-pass active filter, and a programmable gain amplifier [8]. The system has relay control modules by which the power gain and the pre-amplifier stage are controlled based on the certain conditions. If there is any abnormality in the system, preamplifier stage can be isolated from the sensors. Signal conditioning circuits are tested using NI Multisim software before implementation on hardware.

Table.1 Simulated Result for LPF.

For a Single ended Channel			For a differential channel		
Input voltage (V)	Frequency (KHz)	o/p voltage Range in (V)	I/p voltage (V)	Frequency (KHz)	o/p voltage (V)
10V	10	4.72-4.80	200mV	10	4.56-4.72
	33	3.92-4.08		33	3.52-3.60
	35	3.84-4.0		35	3.36-3.52
	38	3.68-3.84		38	3.20-3.28
	40	3.52-3.68		40	3.04-3.12

HDL DESIGN

The chapter gives the overview of the different modules developed in FPGA for interfacing ADC using serial to sample, acquire and send the data. The HDL coding is implemented in VHDL [9]. Serial interfaces are multiplexed on the data bus and eight ADCs are initiated at the same time.

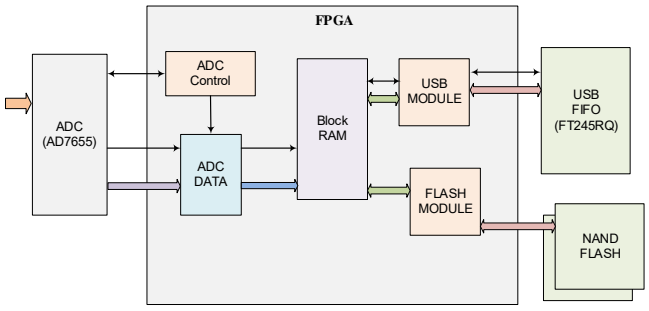

Figure.3. FPGA CONTROL MODULE

Each channel is sampled with 1MSPS sampling rate and the data is given to block RAM. The synchronization between the USB and data is implemented using Block RAM in FPGA. The data stored in Block RAM is

transferred to NAND Flash which is on-board. The data acquired is further processed and sent to Test station PC for further analysis and storage or monitoring [10].

The flow chart shows the software implementation of Data Acquisition System in HDL. When the system is powered ON, the hardware reset goes to the system in the reset state where system is initialized to known initial state. The data should be appended for every power ON to avoid the over write of data previously stored in flash.

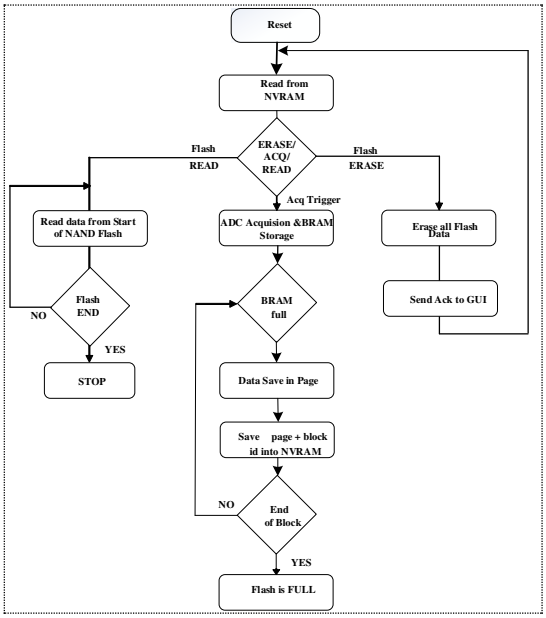

Figure.4. HDL Software Flow

The system is well designed for various field trials to collect the data. NVRAM is used to store the information of flash page and block numbers, time stamp derived from FPGA clock and other critical data for data appending for each power ON. The command from GUI is executed to erase the flash when required to do flash and NVRAM critical data easing. The Acquisition of data or the Download the data is selected by the single ended analog signal. If the signal is more than 4V, the Acquisition is triggered. Otherwise the data stored can be retrieved from the GUI from USB [10]. The data acquired from ADC is stored in the BRAM of FPGA for data writing to Flash. The Page size of flash is 8192Bytes. The data acquired from the ADC are stored in the BRAM along with the derived time stamp from FPGA Clock.

The size of the BRAM is 8KB with input port size of 2Kx32bits and the output port size of 8Kx8bits. If BRAM is full, then the data in BRAM is send to flash page and page number is incremented [11]. The flash page and block number is updated in NVRAM. The data is read from the flash and sent to the USB FIFO to receive the data in PC when flash read command is received from the GUI. End of flash address stored in NVRAM is used to find out if flash data has been downloaded. The FT245R is a USB to parallel FIFO interface device that minimizes the number of external components needed in USB to FIFO design [12].

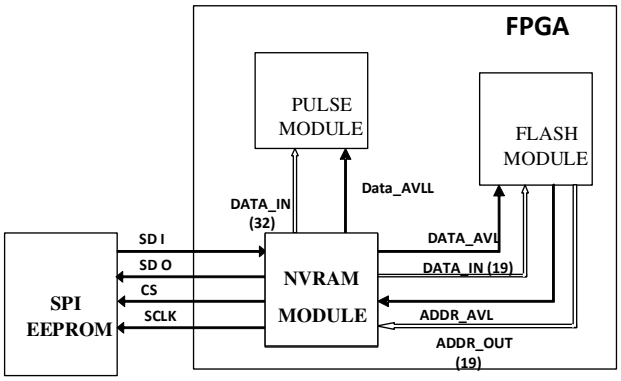

Figure.5. HDL Software Flow

SPI EEPROM is used for storing the critical data whenever it is required. The data transmission is synchronized with the serial clock from FPGA. The rising edge of each serial clock transmits data. The figure.5 shows the interfacing of EEPROM with the FPGA. NVRAM Module in the FPGA is developed to handle the communication between EEPROM and FPGA [13]. Data in the NVRAM is read from it by sending the command word, address and data at the Address is copied to buffer in the memory and it sends the data bit by bit with serial clock. The data contains the time stamp, page and block address for data appending and data downloading. If data from NAND Flash is available, it writes the time stamp, page and block address into EEPROM by sending the command word, address and data bits with the serial clock [1].

The following figure.6 shows the chip scope outputs observed for EEPROM data writing. Whenever the data available signal is high, chip select will be low until the data writing is over.

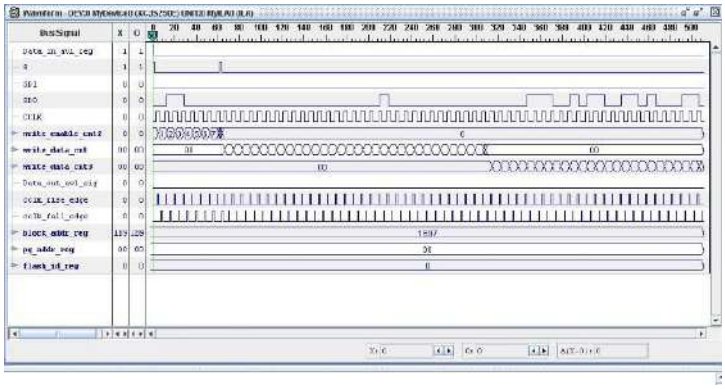

Figure.6. Chip scope results of Nvram Module

The test set-up along with simulation of elements with Test-Jig for flow noise measurement is shown in the figure.7. The system is designed with Virtex-5 FPGA and designed using 8-layer PCB as single card [14]. The differential signals and single ended signals are terminated using shell connectors. Proper care has been taken in designing the system to minimize the noise levels.

The system is fully tested with interfacing the sensors in the tank test by simulating the acoustic signals. The data retrieved is plotted further processed offline to characterize the flow noise. The system is also subjected for field trials to get the flow noise data which was recorded in the flash. The data is retrieved after the test is completed.

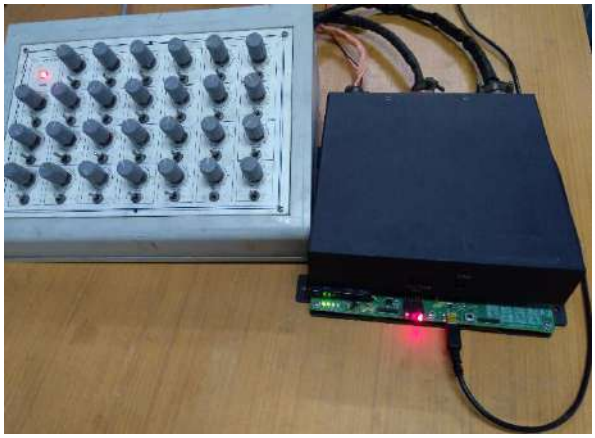

Figure.7. Flow noise Daq with Test set-up

Front End Gui Design

The Graphical User Interface is designed with Visual studio in C++. The software is run in the host PC to get the online data or stored data offline in the frame format. The received data frames are processed and converted into corresponding values for drawing and analyzing acoustic waveforms.

Figure.8. Front end Gui

The necessary drivers for communicating to the Data acquisition systems are integrate and tested through USB. The host PC sends commands to control and process the data in the system. Host PC will get data through USB and the data will be stored in the file while data acquisition is functioning. The data analysis and plotting are set with lower priority as these tasks takes lot of time and memory.

ANALYSIS OF RESULTS

The complete system has been integrated, tested and verified for data acquisition of flow noise in the field trials.

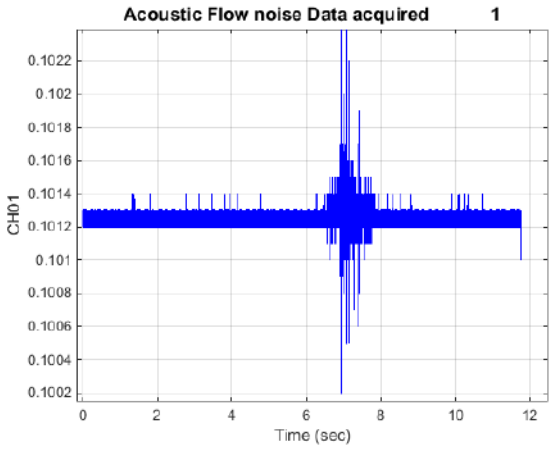

Figure.9. Flow noise data results

Total 32 acoustic sensors are integrated and each channel is sampled at a rate of 100-Kilo samples. As a result, the system achieves a total sampling rate of 3200KSPS, and data is stored and retrieved in nonvolatile flash memory. The flow noise acquired from the sensors is shown in the figure.8.

CONCLUSION

Acoustic data logging and data analysis are significantly enhanced by the multi-channel real-time acoustic data acquisition system. Field trials and high throughput are both possible with the system. The low-power consumption, light weight, and small size of the Data Acquisition System are its greatest advantages. The host PC and front-end communication through USB can be used in the on-board data analysis and communication channel characterization.

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